13th IEEE International New Circuits And Systems Conference (NEWCAS 2015)

June 7-10, 2015

Minatec, Parvis Louis Néel, 38054 Grenoble, France.

http://www.newcas2015.org

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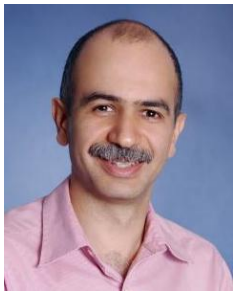

Shahriar Mirabbasi
Technical Program co-Chair

Welcome to NEWCAS 2015

On behalf of the organizing committee, we are very pleased to welcome you to the 13th edition of the IEEE International NEWCAS Conference.

This edition is organized by both CEA-LETI, IMEP-LAHC and TIMA from 7th to 10th of June 2015 in Grenoble. The Conference venue is located at Minatec close to the city center, at the heart of the French Silicon Valley. You will have the opportunity to interact with experts of your domains from all continents and relax while being in the Capital of the Alps. We are confident that your stay will be unforgettable. This year, a total of 326 submissions originating from 52 countries were received.

These were classified thanks to 1100 reviews. This review was carried out efficiently in a short time; we would like to warmly thank all the reviewers.

After a rigorous selection, which guarantees the high level of our conference, 133 regular contributions were scheduled in regular sessions, plus 14 other contributions in 3 special sessions. They were divided in 22 lecture sessions and 2 poster sessions. The acceptance rate for the conference is 41 %. After the conference a journal special issue will be published by Springer in the "Analog Integrated Circuits and Signal Processing" International Journal. The best papers will be extended and selected to appear in this journal. NEWCAS'2015 would not exist without the work of many people. We would like to thank the organizing committee, the Technical Program Committee, the Special Sessions organizers, the Tutorials and Keynote speakers, the reviewers and finally the authors who came to present their work at this NEWCAS edition. We also wish to thank the numerous volunteers that helped the organization, especially the graduate students of CEA-LETI and IMEP-LAHC. We would like also to thank " La Mairie de Grenoble", IMEP-LAHC, TIMA and CEA-LETI for their help. Enjoy NEWCAS'2015 conference and your stay in Grenoble.

Dominique Morche and Mohamad Sawan
General co-Chairs

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Lirida Naviner, Telecom Paritech, France

Track 6: Digital Signal Processing & Multimedia
Yvon Savaria, École Polytechnique de Montréal, Canada
Sergio Bampi, Instituto de Informatica UFRGS, Brazil
Luc Claesen, University Hasselt, Belgium

Track 7: EDA and CAD tools
Marie-Minerve Louërat, CNRS, LIP6, France
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Track8: Energy Harvesting/Scavenging & Power Management
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Track 9: Microsystems, Imaging, Sensors & Actuators
Luc Hébrard, INESS, Université de Strasbourg, France
Maher Kayal, École polytechnique fédérale de Lausanne, Switzerland
Wilfried Uhring, Université de Strasbourg, France

Track 10: Digital Communications
Geneviève Baudoin, ESIEE, France
Christoph Studer, Cornell University, USA

Track 11: Circuits and Systems for Wireless and Wireline Applications
Frédéric Nabki, Université du Québec à Montréal, Canada
José-Luis Gonzalez Jimenez, CEA-Leti, France
Jean-Baptiste Begueret, IMS, Université de Bordeaux, France

Track 12: Embedded and control systems
Suzanne Lesecq, CEA-Leti, France
Michael Huebner, Ruhr-Universität Bochum, Germany

Program at a glance

Sunday, June 7 - Tutorials - PHELMA		
	Amphitheatre 001	**Room 002**
8:30 - 10:00	**1A** Injection Locked Oscillators: Applications, Modeling & Design - Part I	**1B** FDSOI Technology - Part I - Body Biasing techniques in UTBB
10:00 - 10:30	Coffee break	
	Amphitheatre 001	**Room 002**
10:30 - 12:00	**2A** Injection Locked Oscillators: Applications, Modeling & Design - Part II	**2B** FDSOI Technology - Part II - Millimeter Wave 28nm-CMOS FD SOI Power Amplifier Design
12:00 - 13:30	Lunch	
	Amphitheatre 001	**Room 002**
13:30 - 15:00	**3A** Full Software Radio Circuits and Systems: Design by Mathematics in 28nm FDSOI Technology and Application to 5G Standard - Part I	**3B** Substrate Integrated Waveguides: from PCB to Microelectronics Technologies - Part I
15:00 - 15h30	Coffee break	
	Amphitheatre 001	**Room 002**
15:30 - 17:00	**4A** Full Software Radio Circuits and Systems: Design by Mathematics in 28nm FDSOI Technology and Application to 5G Standard - Part II	**4B** Substrate Integrated Waveguides: from PCB to Microelectronics Technologies - Part II
18:30	Welcome reception	

Monday, June 8 - MINATEC Conference Center			
8:30 - 9:10	Auditorium **Opening Ceremony**		
9:10 - 10:10	Auditorium **Plenary Lecture 1, J.Sifakis**		
10:10 - 10:30	Coffee break		
	Auditorium	**Room 222**	**Room 224**
10:30 - 12:00	**7A** Phase Locked Loops and Circuits for Optical Communications	**7B** EDA/CAD tools	**7C** DSP and Multimedia Circuits and Applications
12:00 - 14:00	Lunch		
	Auditorium	**Room 222**	**Room 224**
14:00 - 15:30	**8A** Noise and Random Phenomena in Analog Circuits	**8B** Digital Circuits and Architectures for Processing	**8C** Energy Harvesting: from Devices to Systems
15:30 - 16:30	Coffee break		
15:45 - 17:00	Grand Salon **9A Poster Session I**		**9B Meiji University Students' workshop**
	Auditorium	**Room 222**	**Room 224**
16h30 - 18:00	**10A** Special Session Circuits and Systems for Medical Applications	**10B** Special Session On-chip Measurements for Characterization, Testing, and Calibration of Analog Front-ends and mmW Devices	
18:45	Coktail/Museum visit		

Tuesday, June 9 - MINATEC Conference Center		
9:00 - 10:00	Auditorium **Plenary Lecture 2, C. Fourtet**	
10:00 - 10:30	Coffee break	
10:00 - 11:30	Grand Salon **12A Poster Session II**	
10:30 - 12:00	**Auditorium** **13A** Timing Variations and Resiliency	**Room 222** **13B** Modeling, Design and Conditioning of Sensing Devices
12:00 - 13:30	Lunch	
13:30 - 15:00	**Auditorium** **14A** Wireless Transmitters and Receivers	**Room 222** **14B** Mixed Signal Circuits
15:00 - 15:20	Coffee break	
15:20 - 16:50	**Auditorium** **15A** Voltage References and Power Converters	**Room 222** **15B** Special Session Approximate Computing
16:50 - 18:10	Auditorium **Panel Session**	
18:30	Gala Dinner	

Wednesday, June 10 - MINATEC Conference Center			
9:00 - 10:30	**Auditorium** **17A** Microwave and mm-wave Circuits	**Room 222** **17B** Building Blocks for Biomedical Applications	**Room 224** **17C** Analog-to-Digital Converters
10:30 - 10:50	Coffee break		
10:50 - 11:50	Auditorium **Plenary Lecture 3, B. Nauta**		
11:50 - 13:30	Lunch		
13:30 - 15:00	**Auditorium** **19A** Circuits for Wireless Communications	**Room 222** **19B** Systems for Biomedical Applications	**Room 224** **19C** Special Session Control Techniques for Adaptive Computing Systems
15:00 - 15:20	Coffee break		
15:20 - 16:50	**Auditorium** **20A** Digital Design and Modeling	**Room 222** **20B** Filters and Transconductors	**Room 224** **20C** Sensing Systems Integration
16:50 - 17:20	Auditorium **Closing Ceremony**		

Tutorials

Sunday 7th June 2015, PHELMA

Tutorial 1: "Injection Locked Oscillators: Applications, Modeling, and Design"

Tony Chan Carusone (Integrated Systems Laboratory, University of Toronto, Canada)
Sunday 7th June 2015 from 8:30 to 10:00 (Part I) and from 10:30 to 12:00 (Part II), Amphitheatre 001, Phelma

Abstract
Injection-locked oscillators (ILOs) have experienced increasing use for wireless RF communication and in clocking circuitry for wireline links. This presentation begins with some background on ILOs, highlighting their benefits compared with DLLs, PLLs and other circuitry capable of clock amplification, multiplication, phase generation, interpolation, and phase noise filtering. A challenge limiting the practical use of ILOs in these applications is that their modeling is less well understood. This tutorial will therefore summarize the analysis and practical modeling methods for ILOs. First, the classical linearized model is presented. The intuitive understanding afforded by the linearized model will be highlighted and it will be used to inform high-level design choices. Second, the impulse sensitivity function, a cyclo-stationary approach popularized for modeling phase noise in oscillators, is applied to the modeling of ILOs. Finally, a more accurate model, called the phase transfer characteristic, is described, including methods for model extraction. A live demo of ILO modeling for practical applications will be incorporated into the tutorial using Matlab/Simulink.

The tutorial will then overview the design of ILOs for several practical applications. First, multi-phase clock generation is covered and techniques to ensure uniform spacing of the generated phases are described. Second, the use of ILOs for phase interpolation is discussed. A key challenge here is the ability to provide a clock phase programmable over the entire range ±π radians. For example, some past work in this area has observed that an ILO's performance suffers when used for phase shifts exceeding ±π/2 radians. This problem may be addressed by selectively injecting either the in-phase or quadrature stage of a quadrature ILO, thereby providing an additional 90-degree phase shift. Implementations of this approach are described including both ring and LC oscillators operating at frequencies from 2 - 20 GHz in CMOS technologies from 65nm - 130nm. Finally, approaches towards the design of an ILO for clock multiplication are reviewed. Particular attention is paid to the need to ensure adequate lock range for frequency-agile applications. A useful approach in this regard is to ensure strong injection via multiple sites in the oscillator, demonstrated in a 4x multiplying ILO implemented in 40nm CMOS.
The tutorial will culminate in two detailed design case studies from the presenter's past work that combine multiple ILOs into highly-functional clocking subsystems. First, a high-

frequency jitter-tolerant receiver in 65 nm CMOS is presented. The clock receiver comprises two ILOs to frequency-multiply, deskew, and adjust jitter tracking bandwidth. Jitter tolerance is improved by tracking correlated jitter through the ILOs. Different data rates and latency mismatch between the clock and data paths are accommodated by controlling the ILOs' jitter tracking bandwidth up to 300 MHz. A receiver using this architecture in 65nm CMOS consumes 0.92 pJ/bit operating at 7.4 Gb/s and has a jitter tolerance of 1.5 UI at 200 MHz. Second, a frequency agile multiplying injection-locked oscillator (MILO) suitable for fast power cycling is presented. Edge detectors and multiple injection sites extend the aggregate lock range of two MILOs to 55.7% of the 3.16-GHz center frequency. Monitoring circuits identify the correct MILO and power-off the other within 10 reference clock cycles.

Biography

Tony Chan Carusone received his Ph.D. at the University of Toronto in 2002. Since then, he has been with the Department of Electrical and Computer Engineering at the University of Toronto where he is currently a Professor and the department's Associate Chair, Research. He is a Senior Member of the IEEE, has co-authored the best paper at the 2005 Compound Semiconductor Integrated Circuits Symposium, the best student papers at the 2007, 2008, and 2011 Custom Integrated Circuits Conferences, and the best invited paper at the 2010 Custom Integrated Circuits Conference. He was the Editor-in-Chief of the IEEE Transactions on Circuits and Systems II: Express Briefs and a member of the Technical Program Committee for the International Solid-State Circuits Conference. He currently serves on the editorial board of the IEEE Journal of Solid-State Circuits and on the Technical Program Committee for the VLSI Circuits Symposium. He is a regular consultant to industry in the areas of analog, mixed-signal, and communication integrated circuit design, and is an author, along with David Johns and Ken Martin, of the 2nd edition of the classic textbook "Analog Integrated Circuit Design".

Tutorial 2: "FDSOI Technology"

Philippe Flatresse (STMicroelectronics, Crolles, France), Eric Kerhervé, Aurélien Larie, Baudouin Martineau (IMS Laboratory, Bordeaux, France).

Sunday 7th June 2015, from 8:30 to 10:00 (Part I) and from 10:30 to 12:00 (Part II), Room 002, Phelma

Abstract

- **Part I : Body Biasing techniques in UTBB FDSOI technology**

(by Philippe Flatresse)

With the increasing demand of processing power to be delivered by the System On Chips, it is now key to improve their energy efficiency, not only for thermal or battery life duration purpose but also for environmental considerations such as green supercomputers, wireless base stations and micro servers. Using FD-SOI technology enables designing energy efficient SOCs running at very high frequency over an ultra-wide voltage range while minimizing power dissipation. In this context, STMicroelectronics has developed a full design platform leveraging on body biasing considered as the key design solution to provide best-in class SOCs to the market. The talk will describe the capability of body biasing, showing it is not only well suited for performance boosting but also for power optimization and compensation. Body biasing implementation details will be also shared thru the presentation of several silicon demonstrations.

- **Part II : Millimeter Wave 28nm-CMOS FD SOI Power Amplifier Design**

(by Eric Kerhervé, Aurélien Larie, Baudouin Martineau)

Traditionally, millimeter-wave (mmW) circuits using only III-V technologies have been used in low-volume, high-performance products. With the recent progress of highly scaled Si-based technologies such as 28nm-CMOS FD SOI achieving f_T and f_{max} beyond 300 GHz, the application area of Si-based technologies has broadened from digital, analog, RF, and microwave domains to include mmW applications. The aim of this tutorial is to give the audience the design flow to successful the mmw power amplifier design in 28nm-CMOS FD SOI technology from STMicroelectronics. Recent developments at 60GHz perform by IMS Bordeaux will illustrate this tutorial from a research activity point of view.

Summary of the 60 GHz 28nm-CMOS FD SOI Power Amplifier design flow

- Why CMOS FD SOI?
- PA structure
- Challenge (active device)
- PA operating classes
- Linearity issues in WPAN applications
- Choice of structures and transistor topologies
- 28nm CMOS FD SOI transistor performances
- Optimal transistor finger width for f_{max}
- Optimal biasing for f_T and f_{max}
- Output power and number of transistor fingers
- 28nm CMOS FD SOI transistor design
- Optimum output impedance determination
- Impact of the parasitic interconnections

- Extraction of parasitic elements
- Stability issues
- Impedance matching network design
- Simulation and measurement results of the PA

Biography

Philippe Flatresse received M.S. degree in Electrical Engineering in 1995 and PhD degree in Microelectronics in 1999 from Grenoble institute of technology. During his thesis, he has developed the LETISOI spice model dedicated to SOI technologies at CEA LETI, the R&D laboratory from French Atomic Energy Commission.
In year 2000, he joined STMicroelectronics Central R&D to deploy the SOI digital design within the company. He has developed the first SOI standard cells and SRAM libraries as well as IOs including innovative ESD solutions. He has also invented several dedicated CAD tools and low power digital design techniques such as power switches. Thanks to this work, he has pioneered the SOI technology and demonstrated its key advantages for low power high performance digital applications As a design architect, his current research activities are the exploration, development and implementation of ultra-low power platforms able to work in an energy-efficient way on an ultra-wide range of operating points targeting high-growth application areas. His main objective is to explore the energy efficiency limits of parallel computing on multi-cores systems for ultra-low power processing by combining UTBB FD-SOI technology, advanced power management techniques, hardware accelerators and software infrastructure. His current role in ST is in the specification of the appropriate design solutions and technology variants for CMOS products in the following applications area: multimedia processors, consumer products, servers & routers, gaming, low power microcontrollers. His expertise covers bulk and SOI technologies, high performance energy efficient designs, design of libraries and IPs and silicon qualification. He has authored or co-authored more than 50 technical papers, and has filed more than 10 patents in advanced CMOS technologies.

Eric Kerhervé received the Ph.D. degree in Electrical Engineering from University of Bordeaux, France in 1994. He joined ENSEIRB-MATMECA and the IMS Laboratory in 1996, where he is currently Professor in Microelectronics and Microwave applications. His main areas of research are the design of RF, microwave and millimeter-wave circuits (power amplifiers and filters) in silicon GaAs and GaN technologies. He is or was involved in several European projects (Medea+ UPPERMOST, Medea+ QSTREAM, Catrene PANAMA, FP6 MOBILIS, ENIAC MIRANDELA), to develop silicon RF/mmW power amplifiers. He has authored or co-authored more than 190 technical papers in this field, and was awarded 23 patents. He has organized 8 RFIC and EuMC workshops on advanced silicon technologies for radiofrequency and millimeter-wave applications. He is involved in the technical program committees of various international conferences (ICECS, IMOC, NEWCAS, EuMIC, SBCCI, LASCAS) and he was the general co-chair of the international IEEE ICECS'2006 and IEEE NEWCAS'2011 conferences. He is co-editor of Special Issues for IEEE-ICECS'2006, IEEE-ICECS'2007, IEEE-LASCAS 2010. He was 2-years associate editor of IEEE Transactions on Circuits and Systems II (TCAS II). He is IEEE senior member and member of the IEEE-CAS, IEEE-MTT and IEEE SSCS societies.

Tutorial 3: "Full Software Radio circuits and systems: Design by Mathematics in 28nm FDSOI technology and application to 5G standard"

Yann Deval, François Rivet, Yoan Veyrac, Nassim Bouassida (IMS Laboratory, Bordeaux, France).

Sunday 7th June 2015, from 13:30 to 15:00 (Part I) and from 15:30 to 17:00 (Part II)
Amphitheatre 001, Phelma

Abstract

The diversity of communication standard simplies the use of multi-band and multi-mode radios. Recent years have seen a wide Investigation on Software Defined Radio for Cognitive Radio application. But, this is always constrained to multi---standards prospectives while a complete agility of RF transceivers is required. That is why Full Software Radio proposes to challenge a new way of integrating RF circuits and systems by tackling the main issue: transceiving concurrently any RF signal within a very wide band of interest for telecommunication industry, from 0 to 5GHz for instance.

It is clearlyobserved that disruptive solutions are required. The focus of this tutorial will be on the design by mathematics of such RF transceiver design, exploring novel approaches along with a thorough discussion of advanced techniques for these receivers and transmitters towards a revolution in RF integrated circuits and systems. 28nm FDSOI technology from STMicroelectronics will be detailed to demonstrate its strengths in RFIC design. First, a frequency system is presented using a Sampled Analog Signal Processor as a receiver and a Walsh frequency combiner for the transmitter. Then, a temporal system is presented using a wide-band delta analog to digital converter as a receiver and a RF arbitrary waveform generator, named Riemann Pump for the transmitter. The methodology of every approach will be detailed following the same flow: mathematics, trade-off with RF electronics integration in 28nm FDSOI, architecture proposal, high level simulation results, circuit design issues, measurement results. Finally, an application to 5G standard will be addressed by demonstrating the feasibility of such systems to carrier aggregation, wide-band capabilities, low power consumption and high order of modulation schemes.

Table of content

The goal of this tutorial is to present our original methodology of Full Software Radio system design. The learning objectives address a wide audience:

1. beginner: presentation of RF constraints for circuit design, trade off between specification and 28nm FDSOI technologies.
2. intermediate: analog signal processing issues, noise, power, architecture.
3. advanced: mathematics adequation with transceiver specification, dynamic range, power consumption, technology.

Wireless system designers have been facing the continuously increasing demand for high data rates and mobility required by new wireless applications and therefore have started research on new generation of wireless systems that are expected to be deployed beyond 2020. For instance, 5G wireless networks will support 1,000-fold gains in capacity,

connections for at least 100 billion devices, and a 10 Gbps individual user experience capable of extremely low latency and response times. Deployment of these networks will emerge between 2020 and 2030. We present 3 main techniques:

- SASP Rx is a frequency domain receiver.

The principle of the SASP aims at selecting a spectral envelope of a RF signal within a very wide frequency band. To reach this target, the SASP processes analogically the RF input signal spectrum thanks to an analog Discrete Time Fourier Transform (DFT) with discrete time voltage samples. Once the spectrum is processed, voltage samples representing the spectral signal envelope to be treated are converted into digital. The selection of few voltage samples among thousands replaces the classical mixing and filtering operations. It reduces the A/D conversion frequency from GHz frequencies to MHz ones and thus allows a multi band selection at a very low power consumption. Its application for 5G standard is a direct carrier aggregation to achieve a 1Gbps data rate. SASP is a technique developed by IMS in 2010 by Rivet.

- Walsh is a frequency domain transmitter.

The aim here is to generate any kind of waveform from its spectrum i.e. from its harmonics. For this, and similarly to the Fourier theory, Walsh transform allows decomposing any signal into a series of harmonics. But, instead of building this series on sine waves harmonics, Walsh theorem demonstrates that a family of square waves can generate any kind of signal. Thereby, using a millimeter-Wave [mmW] Phase-Locked Loop [PLL], the harmonic generation can be done at low power and area integration cost. It avoids the integration of several voltage controlled oscillators associated to each harmonics of the series. Indeed, square signals can be generated from a high frequency and divide by 2, N times thanks to a mmW PLL. The mathematical theory based on Walsh theorem states that using algebraic operations (phase shifting, sum, delay, ...) on a finite number of square waves allows to implement this signal generator. The originality of this project is that every square signals are directly amplified and then combined by their power to form the transmitted signal with a correct matching. The sum is performed thanks to a current node. Algebraic operations are consequently carried out by biasing differential amplifying square signals. Walsh is a technique developed by IMS in 2013.

- Riemann Pump is a time-domain transmitter.

The purpose of the Riemann Pump is to generate arbitrary waveforms up to the gigahertz range with a low cost and low consumption solution, the main target being the generation of modulated signals, especially to address the 5G standard. The wanted signal is to be generated thanks to a pre-determined set of slopes. At first, the Riemann code is computed from the theoretical desired signal; it corresponds to the slope index sequence giving the better approximation of the signal (within the meaning of the Riemann integral). This code controls switched current sources, in order to produce current steps that are integrated into an output capacitive load, thus generating a piecewise linear approximation of the wanted signal. Riemann is a technique developed by IMS in 2013.

Biography

Yann DEVAL received his PhD from the University of Bordeaux, France, in 1994. He joined this university in 1993 as an Assistant Professor. In 1999 Pr. Deval became an Associate

Professor and created the IC Design Team at IMS. In 2004 he became a Full Professor at ENSEIRB MATMECA. From 2006 to 2010 Pr. Deval was the head of IC Design Group at IMS. Also, from 2010 to 2012 Pr. Deval was the Director of ALBATROS, the advanced research alliance between THALES and the University of Bordeaux for aeronautics and space applications, and since January 2007 he is the Director of ST IMS collaborative joint research laboratory. He was the General Chair of the 2010 RFIC Symposium in Anaheim, CA, and the General Chair of the 2012 ESSCIRC ESSDERC conferences in Bordeaux, France. Pr. Deval published more than 170 papers in international conferences and journals, and holds 46 patents.

Francois RIVET received the PhD degree in 2009 from the University of BORDEAUX, France. Since June 2010, he is tenured as Associate Professor at Bordeaux Institute of Technology and IMS Lab, the microelectronics laboratory of the University of BORDEAUX. His research is focused on the design of RFICs. Dr. Rivet has publications in top ranked journals (JSSC, TCAS-II), international conferences (RFIC, RWS), national conferences (JNM) and holds 9 patents. He received the Best Paper Award at Software Defined Radio Forum in 2008 at Washington DC, USA.

Yoan VEYRAC received the Master degree in 2012 from the Electrical Engineering School of Bordeaux, France (ENSEIRB-MATMECA). He is currently pursuing the PhD degree at the IMS laboratory (Bordeaux), in the circuits and systems team. He is specialized in RF architectures and circuit design, especially in the field of software radio transmitters.

Nassim BOUASSIDA received the Master degree in 2012 from the University of BORDEAUX, France. He is with STMicroelectronics as a hardware engineer and PhD student at the IMS laboratory (Bordeaux), in the Circuits and Systems team. He is currently working on software radio transmitters.

Tutorial 4: "Substrate Integrated Waveguides: from Early Printed-Circuit Board Processing to Future Smart and Active Material Integration"

Ke WU (Poly-Grames Research Center, Department of Electrical Engineering Center for Radiofrequency Electronics Research of Quebec (CREER), Polytechnique Montréal, Québec, Canada H3T 1J4).

Sunday 7th June 2015, from 13:30 to 15:00 (Part I) and from 15:30 to 17:00 (Part II)
Room 002, Phelma

Abstract

Recent research effort in exploring and exploiting substrate integrated circuits (SICs) has fundamentally changed the landscape of high-frequency circuit and system integration and development. In particular, substrate integrated waveguide (SIW) technology, which is part of the SICs family, has created a great enthusiasm in the applied electromagnetic and integrated circuit community worldwide for a wide range of low cost-enabled commercial and high-performance-oriented defense applications from MHz to THz. The critical enablers in this disruptive technology lie in the successful hybrid and monolithic planarization and integration of non-planar metallo-dielectric waveguides through the structure synthesis made of various processing techniques. The early SIW technology development has been pushed forward and has become matured thanks to the development of a series of single layered and multi-layered printed circuit board (PCB) processing techniques and hybrid multilayered micro-fabrication processing techniques such as LTCC and photo-imageable processing techniques. Those fabrication techniques have contributed to the fast-paced progress of passive integrated components, circuits and antennas. This paper reviews the recent developments and accomplishments of various SIW antenna and circuit techniques with emphasis on PCB-based design platforms. Practical examples are shown for their applications in the design and development of innovative integrated passive circuits and antenna arrays for applications ranging from MHz to THz. Emerging and future development trends of SIW techniques are discussed with special interest in the use and integration of smart and active materials as well as semiconductor-based microelectronic processing techniques such as CMOS schemes over millimeter-wave and terahertz frequency ranges. It is anticipated that emerging CMOS-based "SIW and SICs" will prevail in the decades to come. This presentation will also deal with a number of grand challenging issues and the arising of unprecedented problems in passive-active circuits integrations.

Biography

Ke Wu is Professor of electrical engineering, and Canada Research Chair in RF and millimeter-wave engineering at the Ecole Polytechnique (University of Montreal). He has been the Director of the Poly-Grames Research Center and the Founding Director (2008-2014) of the Center for Radiofrequency Electronics Research of Quebec. He held/holds visiting/honorary professorships at various universities in the world. He has authored/co-authored over 1000 referred papers, and a number of books/book chapters and more than 30 patents. Dr. Wu has held key positions in and has served on various panels and

international committees including the chair of technical program committees, international steering committees and international conferences/symposia. In particular, he was the general chair of the 2012 IEEE MTT-S International Microwave Symposium. He has served on the editorial/review boards of many technical journals, transactions and letters as well as scientific encyclopedia including editors and guest editors. He has been providing consulting services to corporations, governments and universities around the world. Dr. Wu is an elected IEEE MTT-S AdCom member and has served as the chair of many standing committees including Transnational Committee, Member and Geographic Activities (MGA) Committee and Technical Coordinating Committee (TCC). He is the 2015 IEEE MTT-S President-Elect and will become the 2016 IEEE MTT-S President. He also serves as the inaugural North-American representative in the General Assembly of the European Microwave Association (EuMA). He was the recipient of many awards and prizes including the inaugural IEEE MTT-S Outstanding Young Engineer Award, the 2004 Fessenden Medal of the IEEE Canada, the 2009 Thomas W. Eadie Medal from the Royal Society of Canada (The Academies of Arts, Humanities and Sciences of Canada), the Queen Elizabeth II Diamond Jubilee Medal, the 2013 Award of Merit of Federation of Chinese Canadian Professionals, the 2014 IEEE MTT-S Microwave Application Award, the 2014 Marie-Victorin Prize (Prix du Québec – the highest distinction of Québec in the Natural Sciences and Engineering) and the 2015 "Prix d'excellence en recherche et innovation" of Polytechnique Montreal. He is a Fellow of the IEEE, a Fellow of the Canadian Academy of Engineering (CAE) and a Fellow of the Royal Society of Canada. He was an IEEE MTT-S Distinguished Microwave Lecturer from Jan. 2009 to Dec. 2011.

Keynotes speakers

Keynotes 1 :"The Internet of Things – The Ultimate ICT Revolution"

Joseph Sifakis - CRI Grenoble, Professor at EPFL

Monday, June 8th from 09:10 to 10:10 Auditorium, Minatec

Abstract

The Internet of Things (IoT) is a vision born from the convergence between embedded and networking technologies. It refers to the interconnection of uniquely identifiable embedded computing devices within the existing Internet infrastructure. Things can refer to a wide variety of devices such as heart monitoring implants, biochip transponders, automobiles with built-in sensors, field operation devices, smart thermostat and home appliances. They are equipped with sensors, actuators and microcontrollers which can provide the "real-time" embedded processing that is a key requirement of most IoT applications. The collected data are made available through a unified networking infrastructure, to users and interconnected machines. Furthermore, they can be processed and analyzed by the cloud for decision-making in order to respond to changes quickly and accurately, to predict events and optimize resources.

We shortly discuss the IoT vision and its feasibility. We show that its achievement challenges our capacity to design mixed hardware-software systems that are trustworthy and optimal. We advocate the need for rigorous system design techniques. We present the current state of the art and discuss three major scientific problems: 1) linking physicality and computation; 2) component-based systems engineering; 3) intelligence in particular as the ability of system adaptation in order to meet given requirements in the presence of uncertainty.

Achieving the IoT vision will have a tremendous societal, technological and scientific impact. In particular, it will reinvigorate Computing and enrich the discipline with new scientific foundations.

Joseph Sifakis – Short Bio

Joseph Sifakis is Emeritus Senior Researcher at CNRS, full professor at Ecole Polytechnique Fédérale de Lausanne (EPFL) and the director of "Centre de la Recherche Intégrative" (CRI) in Grenoble. His current research interests cover fundamental and applied aspects of embedded systems design. The main focus of his work is on the formalization of system design as a process leading from given requirements to trustworthy, optimized and correct-by-construction implementations. Joseph Sifakis is the founder of the Verimag laboratory in Grenoble, which he directed for 13 years. Verimag is a leading research laboratory in the area of embedded systems, internationally known for the development of the Lustre synchronous language used by the SCADE tool for the design of safety-critical avionics and space applications. In 2007, Joseph Sifakis has received the Turing Award for his contribution to the theory and application of model checking, the most widely used system verification technique today. Joseph Sifakis has had numerous administrative and managerial responsibilities both at French and European level. He has actively worked to organize the European research community in embedded systems as the scientific coordinator of the « ARTIST » European Networks of Excellence, for ten years. He has participated in many major industrial projects led by companies such as Airbus, EADS, France Telecom, Astrium, and STMicroelectronics.

Joseph Sifakis is a member of the French Academy of Sciences, a member of the French National Academy of Engineering and a member of Academia Europea. He is a Grand Officer of the French National Order of Merit, a Commander of the French Legion of Honor. He has received the Leonardo da Vinci Medal in 2012.

Keynotes 2: "Circuit Techniques for next Generation Wireless Communication"

Bram Nauta - University of Twente, The Netherlands

Wednesday, June 10th from 10:50 to 11:50

Auditorium, Minatec

Abstract

Due to the increase of wireless standards using different RF frequencies there is a need to have transceivers that can handle a wide range of RF frequencies.

By abandoning the classical narrowband approach, new receiver architectures are explored in which noise and interferer robustness problems have to be solved. At the same time new features are wanted such as spectrum sensing for cognitive radio and self-interference cancelling for future full duplex communication. In this presentation several circuit and system techniques will be illustrated that may enable future radio systems.

Bram Nauta – Short Bio

Bram Nauta was born in 1964 in Hengelo, The Netherlands. In 1987 he received the M.Sc degree (cum laude) in electrical engineering from the University of Twente, Enschede, The Netherlands. In 1991 he received the Ph.D. degree from the same university on the subject of analog CMOS filters for very high frequencies. In 1991 he joined the Mixed-Signal Circuits and Systems Department of Philips Research, Eindhoven the Netherlands. In 1998 he returned to the University of Twente, as full professor heading the IC Design group. His current research interest is high-speed analog CMOS circuits, software defined radio, cognitive radio and beamforming.

He served as the Editor-in-Chief (2007-2010) of the IEEE Journal of Solid-State Circuits (JSSC), and was the 2013 program chair of the International Solid State Circuits Conference (ISSCC). Also he served as Associate Editor of IEEE Transactions on Circuits and Systems II (1997-1999), and of JSSC (2001-2006). He was in the Technical Program Committee of the Symposium on VLSI circuits (2009-2013) and is in the steering committee and programme committee of the European Solid State Circuit Conference (ESSCIRC). Moreover he is member of the ISSCC Executive committee. He served as distinguished lecturer of the IEEE, is elected member of IEEE-SSCS AdCom and is IEEE fellow. He is co-recipient of the ISSCC 2002 and 2009 "Van Vessem Outstanding Paper Award" and in 2014 he received the 'Simon Stevin Meester' award (500.000€), the largest Dutch national prize for achievements in technical sciences. In the same year he has been appointed as distinguished professor at the University of Twente.

Keynotes 3: "The technical challenges of future IoT networks and their consequences on modem's and SoC's design"

Christophe Fourtet - SigFox, France

Tuesday, June 9th from 9:00 to 10:00

Auditorium, Minatec

Abstract

IoT or « Internet of Things », recognized as the future massive extension of "M2M", will become one of the major markets of the following years and is going to bring incredible revolutions in industrial, and generally speaking, human activities, like energy, resource management, necessary replacement of programmed obsolescence by predictive maintenance or "on demand improvements" of machines, health care improvements, optimized agriculture...etc...

For those revolutions to come true, beyond necessity of other ongoing breakthrough on materials, nano-tech, or sensors, the IoT telecom revolution itself needs to be a reality. This is the big challenge. Because an unprecedented density of devices, at very low cost, with outstanding needs for autonomy, that humanity will have to "forget" along their service after "dissemination" on the field, will require a complete "flip-over" of the philosophy that has been dominating in the telecom industry for 100 years, with a culminating point in modern radiotelephony and internet.

Networks are today massively forcing their "administrated" modems to be highly disciplined (in frequency or modulation accuracy, time synchronization...) before they can negotiate a single bit of data. For a working IoT world, networks will need to be switched to "highly cognitive", with a high capacity to dynamically adapt to the various behavior of the disseminated devices they will have to "serve", through massively parallel Software Defined principles.

"Networks at the service of free devices" : A true historic revolution in telecoms in fact !

Those philosophy changes will have unprecedented consequences on the modem's properties that will be embedded in those famous "objects", and thus will have consequences on hardware as well as software components from which they will be built. By cascade effect, consequences on SoC definition and design, will not be of minor importance…

Christophe Fourtet – Short Bio

Graduated from INSA de Lyon and holds a DEA in electromagnetism, Christophe Fourtet is a long time enthusiast of science and technology, particularly radio and electromagnetism. This passion will take him to work on multiple radio projects in companies such as Thomson, TALCO, SAGEM, MOTOROLA, as a design engineer and as a technical manager. He has been working on topics such as PMR, then pioneering digital PMR as well as digital cellular, and then 3G / LTE. In fact, caught in the 90s as many radio specialists by the wave of cellular and its quest of broadband, he made a 180 degree turn starting to work on more "frugal" and "low footprint" radio systems, combining low power and high performance for a given service.

The modern UNB (Ultra Narrow Band) began to be born, and it is his meeting with Ludovic Le Moan, that triggered the spark of SIGFOX five years ago.

Special Sessions

1 - CIRCUITS AND SYSTEMS FOR MEDICAL APPLICATIONS

Organizers: Dr. Guillaume Charvet (CEA, France)

Monday June, 8th, from 16:30 to 18:00, Room Auditorium

Abstract:
Recent advances in the field of integrated circuits design and systems have been open new opportunities for the design of innovative medical devices. This special session focuses on the design of medical devices based on innovative circuits and the targeted medical applications.

The design of medical devices needs to respect a lot of constraints such as ultra-low power, miniaturization, safety and reliability. Moreover, in order to go to clinical trials, the medical device needs to satisfy all the regulatory requirements. Taking into account all these constraints at the earliest in the design of a medical device is essential.

Likewise, this special session aims to provide a vision of the future needs of technological bricks and the associated constraints, in order to design the future generations of medical devices.

Papers:

"Low-Power Radar Techniques for Remote Sensing and Detection of Vital Signs"
K. Wu
University of Montreal, Canada

"A wireless fully implantable ECoG recording medical device WIMAGINE®: from the design of an integrated circuit toward a clinical trial"
G. Charvet, C. Mestais, F. Sauter-Starace, M. Foerster, A. Lambert, C. Chabrol, S. Robinet, R. D'Errico, V. Josselin, N. Torres-Martinez, T. Costecalde, D. Ratel, A.L. Benabid
CEA-LETI, Grenoble, France

"Advanced Active Implantable Medical Devices how to get the best trade off between research needs and clinical usability"
D. Guiraud (IEEE EMBS Member), G. Cathébras (IEEE Member), D. Andreu
INRIA, Montpellier University, France

2- ON-CHIP MEASUREMENTS FOR CHARACTERIZATION, TESTING, AND CALIBRATION OF ANALOG FRONT-ENDS AND MMW DEVICES

Organizers: Jean-Daniel Arnould (IMEP-LAHC); Haralampos-G. Stratigopoulos (TIMA Labs, France)

Monday June, 8th, from 16:30 to 18:20, Room 222

Abstract:
The purpose of the special session is to discuss state-of-the-art on-chip measurement methods in the context of characterization of mmW devices and testing and calibration of analog, mixed-signal, and RF integrated circuits. The need for low-overhead, non-intrusive, and reliable on-chip measurement methods is dictated by (a) the heterogeneity and complexity of modern mixed analog-digital systems-on-chip and systems-in-package that offer very limited controllability and observability from the output pins in order to perform testing; (b) the increased process variations in advance technology nodes (e.g. 65nm and beyond) that make post-manufacturing calibration of outmost importance in order to correct yield loss; (c) safety-critical and mission-critical systems that need to be equipped with on-chip self-calibration mechanisms for detecting early reliability hazards and applying self-corrective actions (e.g. fault tolerance, self-repair, etc.); and (d) the numerous modern applications of high-frequency devices (e.g. RF, mmW) whose accurate characterization and post-silicon verification requires to rely on on-chip test structures, since extracting signals off-chip for processing seriously degrades the measurement accuracy. This special session will gather together worldwide experts on the above research fields to share with the conference attendees the most recent and state-of-the-art solutions proposed to date.

Papers:

"Self-healing of RF circuits using built-in non-intrusive sensors"

Martin Andraud, Haralampos-G. Stratigopoulos, and Emmanuel Simeu,
TIMA Laboratory, Grenoble, France

"150 GHz load pull measurements on BiCMOS 55nm SiGe:C HBT using in situ tuner "

Alice Bossuet[1,2,3], Thomas Quemerais[2], Estelle Lauga-Larroze[1], Jean-Michel Fournier[1], Christophe Gaquière[3]
[1] IMEP-LAHC, France
[2] STMicroelectronics, France
[3] IEMN, France

"Integrated Test Concepts for In-Situ Millimeter-Wave Device Characterization "

D. Kissinger [1,2], J. Nehring [3], A. Oborovski [3], K. Borutta [3], I. Nasr [4], B. Laemmle [5], R. Weigel [3]
[1] IHP, Im Technologiepark Frankfurt, Germany
[2] Technische Universität Berlin, Berlin, Germany
[3] Institute for Electronics Engineering, Erlangen, Germany
[4] Infineon Technologies, Neubiberg, Germany
[5] Intel, Neubiberg, Germany

"Embedded Instruments for Enhancing Dependability of Analogue and Mixed-Signal IPs"

Jinbo Wan and Hans G. Kerkhoff
TDT, CTIT, University of Twente, Netherlands

"Substrate-Coupling effect in BiCMOS technology for millimeter wave applications"

S. Fregonese[1], R. D'Esposito[1], M. De Matos[1], A. Köhler[2], C. Maneux[1], T. Zimmer[1] (IEEE Member)

[1] CNRS-UMR 5218, University of Bordeaux, Talence, France.

[2] Franhöfer Institute, Dresden, Germany

"Calibration and Characterization Techniques for On-Wafer Device Characterization."

L. Galatro and M. Spirito,

Electronics Research Laboratory/DIMES, Delft University of Technology, Delft, The Netherlands

3- APPROXIMATE COMPUTING

Organizers: Prof. Amara Amara (ISEP, Paris), Prof. Andreas Burg (EPFL, Lausanne)

Tuesday June, 9th, from 15:20 to 16:50, Room 222

Abstract:

Motivation: CMOS technology is approaching its physical limits which manifests itself in diminishing returns from scaling in terms of speed and power consumption. Furthermore, reliability issues and uncertainties require more and more overhead for protection and larger guardbands to always ensure 100% reliable operation.

Topic: Approximate computing is a brand new design paradigm that has recently emerged as a potential solution to i) provide further improvements in speed and energy efficiency beyond scaling and ii) to deal with variability and reliability issues in advanced process nodes. While approximate computing comprises a wide range of techniques and ideas, it generally refers to the principle of relaxing the accuracy requirement on computations based on circuit-level considerations. Due to its highly vertical nature, the topic is extremely interdisciplinary and appears in a wide range of research communities, ranging from devices to VLSI circuits and architectures, to design automation/CAD, all the way to signal processing. Need for a special session at NEWCAS: In particular, in the design automation community, approximate computing and the issues related to reliability and variability have emerged over the last 3-4 years as one of the most prominent topics. Design automation conferences usually have corresponding tracks that discuss related design methodologies. However, we believe that there is also a very important circuit and systems component that is a very good match with the target audience of the NEWCAS conference. To highlight and discuss this component, we propose this special session for NEWCAS 2015 with a number of contributions from well-known experts in the field.

Papers:

"A Scalable Model for Timing Error Prediction under Hardware and Workload Variations "

X. Jiao[1], A. Rahimi[1], B. Narayanaswamy[1], H. Fatemi[2], J. Pineda de Gyvez[2], and R. K. Gupta[1]

[1]CSE, UC San Diego, [2]NXP Semiconductors

"Approximate Computing with Unreliable Dynamic Memories"

S. Ganapathy[1] A. Teman[1] R. Giterman[2] A. Burg[1] G. Karakonstantis[3]

[1] EPFL, Switzerland

[2] ENICS Lab, Faculty of Engineering, Bar Ilan University, Ramat Gan, Israel

[3] High Performance and Distributed Computing, Queen's University Belfast, UK

"Energy Efficient Digital Design through Inexact and Approximate Arithmetic Circuits"

Vincent Camus, Jeremy Schlachter, Christian Enz
EPFL, Switzerland

"Near-Threshold Computing for Very Wide Frequency Scaling: Approximate Adders to Rescue Performance"

Soares, L. B.[1]; Bampi, Sergio[1,2]; Rosa, A.L.R[2]; Costa, E.A.C[3].
[1] Graduate Program on Microelectronics (PGMicro)
[2] PPGC - Informatics Institute
Federal University of Rio Grande do Sul (UFRGS)
[3] Catholic University of Pelotas (UCPEL)
Porto Alegre, Brazil

"Stochastic Computation With Spin Torque Transfer Magnetic Tunnel Junction"

L. Alves de Barros Naviner[1], H. Cai[1], Y. Wang[1], W. Zhao[2,3], A. Ben Dhia[1]
[1] Institut Mines-Telecom, Telecom-ParisTech, Paris, France
[2] IEF, Univ. Paris-Sud 11, Orsay, France
[3] Beihang University, China

4- CONTROL TECHNIQUES FOR ADAPTIVE COMPUTING SYSTEMS

Organizers: Edith Beigné, Suzanne Lesecq, Anca Molnos (CEA, France)

Wednesday June, 10th, from 13:30 to 15:00, Room 224

Abstract

Today mobile systems face strong constraints, especially regarding power consumption and thermal aspects while their performances are still increasing. To answer these new challenges, designers of circuits (analog, digital and mixed-signal, but also RF, MEMS) implement their circuits with some "adaptivity" features. For instance, part of the circuit will automatically adapt its parameters in order to reach the most effective functioning point from a performance versus consumption point of view. Dynamic Voltage and Frequency Scaling techniques can be seen as adaptive approaches that provide to the circuit just enough energy to perform the task it has to do, no more! However, advanced technologies, e.g. FDSOI ones, enlarge the design and functioning space with new parameters to be fixed either at design-time or at run-time. Other teams try to implement event-based approaches in order to make the circuit working only when mandatory.

However, these adaptive capabilities may have counterproductive effects if their design does not take into account (among others) stability and robustness issues. Techniques from the control community may help to answers these issues. The special session will provide an overview of such control techniques applied to adaptive systems, especially, but not limited to, regarding resource management, adaptable middleware, automatic control methods for energy/power reduction, seamless reconfiguration of algorithms and computing systems.

Papers

"Energy-efficient control through power mode placement with discrete DVFS and Body Bias",

Y. Akgul[1], D. Puschini[1], L. Vincent[2], P. Benoit[3], M. Altieri-Scarpato[1]
[1] CEA, LETI, Grenoble, France
[2] Labex PERSYVAL-Lab, Grenoble University
[3] LIRMM, University of Montpellier 2, Montpellier, France

"A distributed synchronization of all-digital PLLs network for clock generation in synchronous SOCs",

C. Shan[1], E. Zianbetov[1], F. Anceau[1], O. Billoint[2], D. Galayko[1]
[1] Laboratoire d'informatique de Paris 6 (LIP6) – University of Pierre and Marie Curie (UPMC), Paris, France
[2] CEA-LETI, Grenoble, France,

"Adaptive Computing in Real-Time Applications",

B. Janßen, F. Schwiegelshohn, M Hübner
Embedded Systems for Information Technology, Ruhr-University Bochum, Bochum, Germany

"Autofocus performance realization using automatic control approach",

M. Zarudniev[1], A. Tonda[1], L. Alacoque[1], S. Bolis[2], A. Pouydebasque[2], F. Jacquet[2]
[1] CEA-LETI Grenoble, France
[2] Wavelens, Grenoble, France

"WSN Power Management with Battery Capacity Estimation",

O. Mokrenko[1], M.-I. Vergara-Gallego[1], W. Lombardi[1], S. Lesecq[1], C. Albea[2]
[1] CEA, LETI, Grenoble, France
[2] CNRS, LAAS, Toulouse France

MEIJI UNIVERSITY STUDENTS'WORKSHOP

Monday, June 8th from 15:45 to 17:00, room Grand Salon

The NewCAS 2015 conference runs the 3rd Edition of the ISEP-Meiji University students' workshop.

This workshop aims to support the cooperation between both institutions and to develop skills and competences needed in the research field for graduate students. The students follow the entire resarch flow: bibliographic study, research work, paper writing, poster/slides preparation and presentation in English are a good way to attract talent in research.

This year, eleven students from Meiji University and two PhD students from ISEP will present their research works during NEWCAS poster sessions. Their research topics include, but are not limited to analog filters, VCO, UWB radar, radio communication systems, Amplifiers…

The NewCAS organizing committee invites all attendees to visit this students' workshop and to discuss with the authors.

Panel Session

IoT Revolution :
What is the key enabler ?
Technology, Software or Application

Tuesday, June 9th 2015 from 16:50 to 18:10, Auditorium, Minatec

Panel Moderator:

- Didier Belot (*Engineer, CEA LETI*)

Panelists:

- Joseph Sifakis (*Director, EPFL*)
- Yann Deval (Professor, *IMS*)
- Bram Nauta (*Professor, UNIVERSITY OF TWENTE*)
- Christophe Fourtet (*CTO, SigFox*)
- Remy Pottier (*Director, ARM*)

Abstract:

The **Internet of Things** (**IoT**) is the network of physical objects or "things" embedded with electronics, software, sensors and connectivity to enable it to achieve greater value and service by exchanging data with the manufacturer, operator and/or other connected devices. Each thing is uniquely identifiable through its embedded computing system but is able to interoperate within the existing Internet infrastructure." This is the definition given by "Wikipedia".

Could we have a look on key words embedded in this definition?

The **things** are globally any objects, (any animal? Any persons?), which is connected to the web through a wireless (or rarely wireline) **connectivity** exchanging **Private or Public data,** coming from **physical sensors** with or without **soft post processing,** with **other Internet users.**

A list of questions coming from this definition are opened:

How can we supply such devices which are not plugged?
How can we sort out the good data to be sent, to be stored?
How can we manage the multiple connectivity standards?
How can we guaranty the privacy?
Where will be stored the information?
How can we reduce the global consumption increasing connected devices?
Which application(s) will be the driver of such network?
What will be the public acceptance, and why?

Finally which will bring the answer to these questions, the technology? The Software? The applications? A mix of all? Or other Key enablers?

General information

Registration desk schedule

Registration desk on site will be opened:
Sunday, June 7th 2015, from 8:00 to 17:00 at Phelma
Monday, June 8th 2015, from 8:00 to 18:00 at Minatec
Tuesday, June 9th 2015, from 8:30 to 18:00 at Minatec
Wednesday, June 10th 2015, from 8:30 to 17:00 at Minatec

Workshop Tutorial

Sunday, June 7th 2015: Phelma Minatec

Information

Any request for information of a general nature can be addressed to registration desk. Messages can be left at the registration desk; delegates will not be disturbed during the session excepted for emergencies.

Technical support

Every room is equipped with a computer and a LCD projector. Should you need any technical assistance, please contact the registration desk prior to your presentation. For oral presentation a station will be set up to test your presentation files.

Special notes for presenters

To ensure smooth running sessions, we recommend the following:
Lecture presenters must be present in the session room at least 10 minutes before the beginning, and the presentation files must be loaded onto the computer before the session starts. Each presentation will last 15 minutes followed by a 3 minutes period to allow for questions and brief discussions.
Poster presenters must have their poster set-up and removed according to the schedule of the sessions they have been assigned to.

Poster set-up and removal schedule

Monday, June 8th 2015:
Set-up: 15:00 to 15:30
Removal: 17:00 to 17:30

Tuesday, June 9th 2015:
Set-up: 8:30 to 10:00
Removal: 11:30 to 13:00

Special events of this conference

Outdoor activity "Acrobastille": close to the "restaurant du téléférique", La Bastille, *Sunday, June 7th 2015 between 18:00 to 19:30*.
Discover the Fort with a zip-line overflying the fortifications, and overcome balance games traps: certainly the best introduction to Grenoble! Please note that sportswear and trainers are recommended and that, if you're afraid of heights, you might jump directly to the welcome cocktail!

Welcome reception: "restaurant du téléférique", La Bastille, *Sunday, June 7th 2015 at 19:00*
From the terrace, enjoy the view over the whole city and don't forget to hydrate yourself! Note that the cable car will close at 21:00.

Opening ceremony: Minatec, *Monday, June 8th 2015 between 09:10-10:10*

Coktail/museum visit: Musée de Grenoble, *Monday, June 8th 2015 at 18:45*
From 18:45 to 19:30 : Guided tour of the gallery
From 19:30 to 20:30 : Welcome speech by Mr le Maire de Grenoble and buffet

The NEWCAS 2015 cocktail will take place at Grenoble Museum. With its collections of ancient, modern and contemporary art, the Musée de Grenoble offers you a chance to traverse the history of western painting from the 13th to the 20th centuries. Included are major masterpieces of classical Flemish, Dutch, Italian and Spanish painting; one of 20th century Europe's richest collections.

All the NEWCAS 2015 attendees will have the opportunity to discover an exceptional temporary exhibit, entitled *From Picasso to Warhol,* where the museum exposes its last acquisitions of the decade. The exhibition present a collection, wealthy and varied, of 150 works of different types as paintings, sculptures, photographs... Mainly of the 20th century but also other previous works. The two focal points of the exhibition are obviously *Verre* (1914) -a rare cubist collage- by Picasso and *Jackie* by Warhol. However, there are many other interesting works of art in the gallery that guides will present you.

Gala dinner: Chateau de Sassenage, Tuesday, *June 9th 2015 at 19:00*

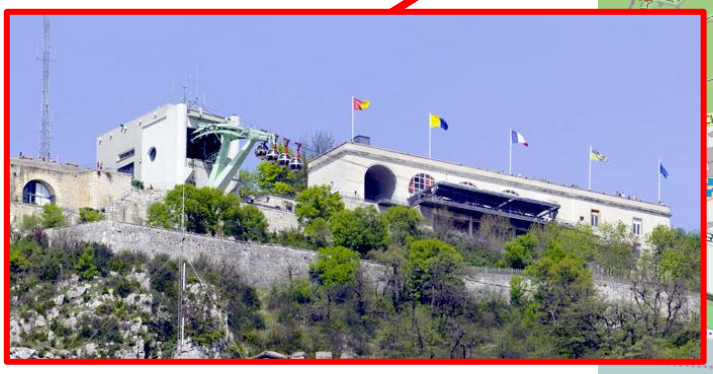
Closing ceremony: Minatec, Wednesday, *June 10th 2015 between 16:50-17:20*

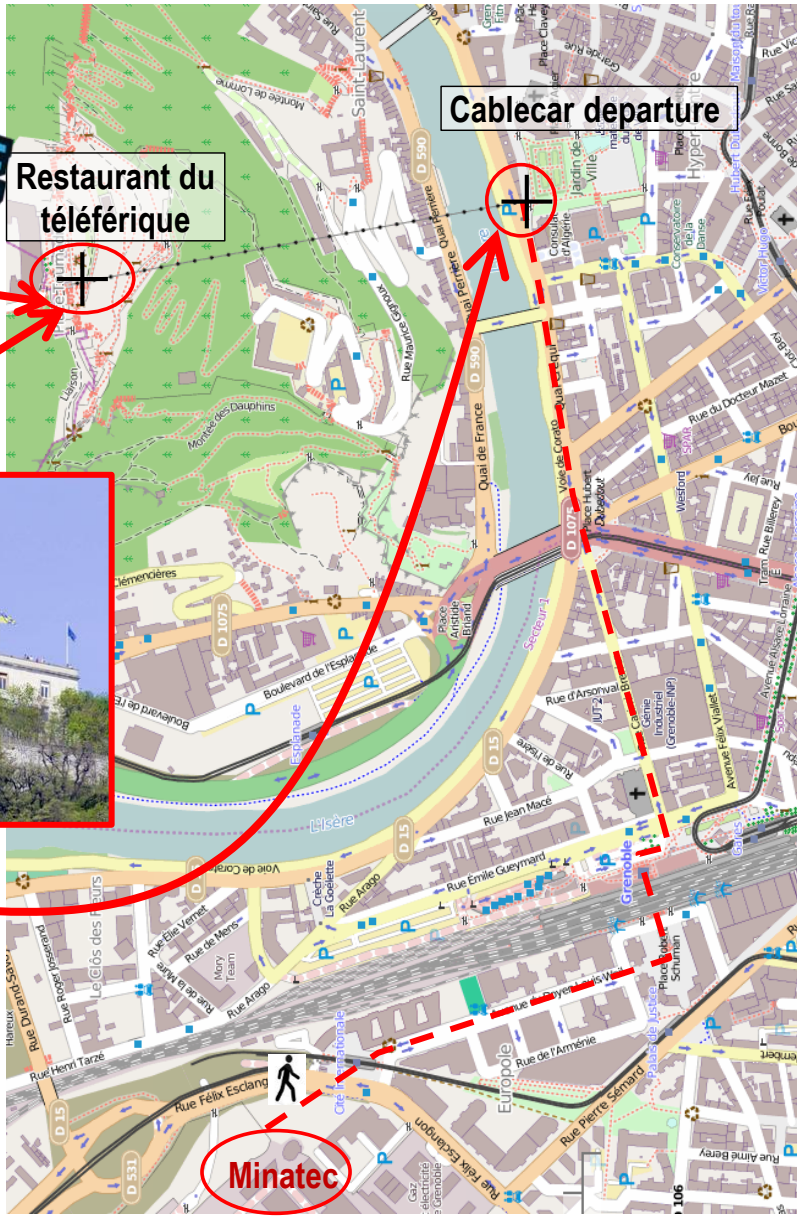
Outdoor activity "Acrobastille" / Welcome reception

"La Bastille" Restaurant du téléférique
Sunday, June 7th 2015 at 19:00

"La Bastille". It is a small fortified mountain located at the crossroad of three valleys, served by the first urban cable-car in the world. There you will discover the flattest town in France in its mountain setting! When the sunsets and the lights go down in the city, the view is outstanding

How to go to La Bastille: you can take the cablecar, Quai Stéphane Jay, 15 minutes walk from Minatec. "Les bulles" (nickname of the cablecar) will take you to the top of the hill, 20 meters from the "restaurant du téléférique". Note that, before 17:30, cablecar tickets can be withdrawn at the conference registration desk.





Coktail / Museum visit

Grenoble Museum
Monday, June 8th 2015 at 18:45
Sponsored by the town council "Mairie de Grenoble"

With its collections of ancient, modern and contemporary art, the Musée de Grenoble offers you a chance to traverse the history of western painting from the 13th to the 20th centuries. Included are major masterpieces of classical Flemish, Dutch, Italian and Spanish painting; one of 20th century Europe's richest collections.

To go to the Cocktail/Museum

By tram:

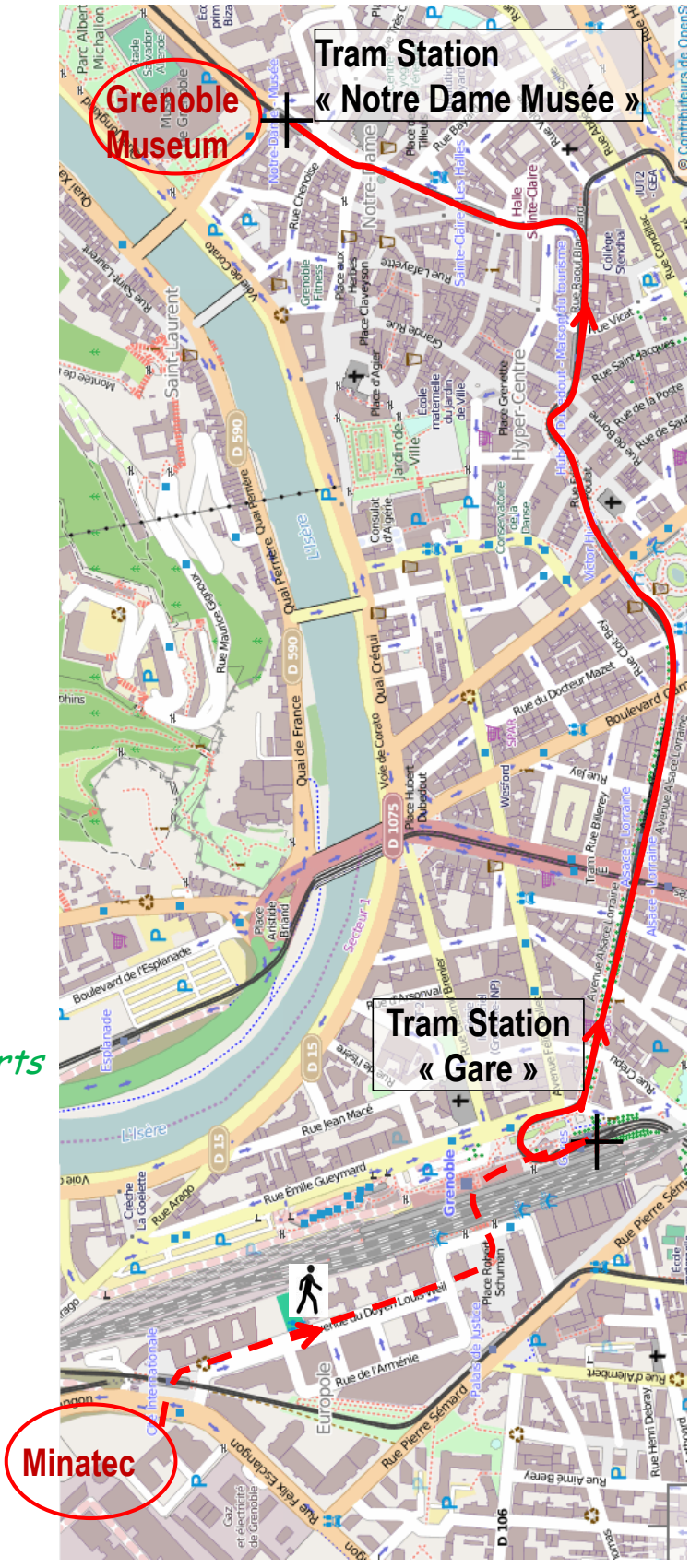
Take the tram B

at the tram station "Gares"

in direction of *Gières-plaine des sports*

Stop at the tram station

"Notre Dame Musée"



Gala Dinner

Château de Sassenage
Tuesday, June 9th 2015

The NEWCAS 2015 Gala dinner will take place on Sassenage Castel.

Built in the 17th century by Charles Louis Alphonse de Sassenage, this classic architecture castle is the last of three houses built by the powerful lords of Sassenage. Work of the architect Laurent Valence Summary, reflects the lifestyle of the Grand Century grandeur and magnificence which rhyme with sweetness and joy of living. The site, consisting of the castle and its landscaped grounds of the 19th century, is classified as a historical monument.

Sassenage Castel is 7km from Minatec so you will have to take buses to join the Gala Dinner. Buses will leave at 18:30 from the parking situated close to Minatec (as indicated in the map below).

A drink will be served in the castel garden. You will then be enjoying the delicious french cuisine. Good music (with the famous group : Nuage de Swing) and excellent french wine will be there for our great party so don't miss it.

To go to the Gala dinner:

Transportation to the "Château de Sassenage" will be available.

Buses will depart from Minatec at 18:30.

Technical program

Sunday, June 7th

LOCATION: PHELMA Engineering School.

08:30-10:00 Session 1A: Tutorial 1 - Injection Locked Oscillators: Applications, Modeling, and Design - Part I

LOCATION: Amphitheatre 001

Tony Chan Carusone

University of Toronto

08:30-10:00 Session 1B: Tutorial 2 - FDSOI Technology - Part I - Body Biasing techniques in UTBB

LOCATION: Room 002

Philippe Flatresse

ST Microelectronics

10:00-10:30 Coffee Break

10:30-12:00 Session 2A: Tutorial 1 - Injection Locked Oscillators: Applications, Modeling, and Design - Part II

LOCATION: Amphitheatre 001

Tony Chan Carusone

University of Toronto

10:30-12:00 Session 2B: Tutorial 2 - FDSOI Technology - Part II - Millimeter Wave 28nm-CMOS FD SOI Power Amplifier Design

LOCATION: Room 002

Eric Kerhervé, Aurélien Larie, Baudouin Martineau

IMS

12:00-13:30 Lunch Break

13:30-15:00 Session 3A: Tutorial 3 - Full Software Radio Circuits and Systems: Design by Mathematics in 28nm FDSOI Technology and Application to 5G Standard - Part I

LOCATION: Amphitheatre 001

Yann Deval, François Rivet, Yoan Veyrac, Nassim Bouassida

IMS

13:30-15:00 Session 3B: Tutorial 4 - Substrate Integrated Waveguides: from PCB to Microelectronics Technologies - Part I

LOCATION: Room 002

Ke Wu

Polytechnique Montréal

15:00-15:30 Coffee Break

15:30-17:00 Session 4A: Tutorial 3 - Full Software Radio Circuits and Systems: Design by Mathematics in 28nm FDSOI Technology and Application to 5G Standard - Part II

LOCATION: Amphitheatre 001

Yann Deval, François Rivet, Yoan Veyrac, Nassim Bouassida

IMS

15:30-17:00 Session 4B: Tutorial 4 - Substrate Integrated Waveguides: from PCB to Microelectronics Technologies - Part II

LOCATION: Room 002

Ke Wu

Polytechnique Montréal

18:00-19:30 Welcome reception – La Bastille

Monday, June 8th

LOCATION: Minatec Conference Center

08:30-09:10 Opening Ceremony

LOCATION: Auditorium

09:10-10:10 Session 6: Plenary Lecture J. Sifakis

LOCATION: Auditorium

SESSSION CHAIR: M. Belleville – *CEA-LETI*

Joseph Sifakis

The Internet of Things – The Ultimate ICT Revolution

EPFL

10:10-10:30 Coffee Break

10:30-12:00 Session 7A: Phase Locked Loops and Circuits for Optical Communications

LOCATION: Auditorium

SESSSION CHAIR: R. Lababidi - *IM2NP,* F. Hameau – *CEA-LETI*

7A1 *Anh Chu*, *Navneeta Deo*, *Waqas Ahmad*, *Markus Törmänen* and *Henrik Sjöland*

An Ultra-low Power Charge-Pump PLL with High Temperature Stability in 130 nm CMOS

Lund University

7A2 *Khaldoon Abugharbieh* and *Karam Gharbieh*

A 20 Gbps Voltage Mode Transmitter with a High-Frequency Signal Boost in 28nm CMOS Technology

Princess Sumaya University for Technology

7A3 *Konstantinos Moustakas* and *Stylianos Siskos*

Low Voltage CMOS Charge Pump with Excellent Current Matching Based on a Rail-to-Rail Current Conveyor

Aristotle University of Thessaloniki

7A4 *Robert Polster*[1], *José Luis Gonzalez-Jimenez*[1] and *Eric Cassan*[2]

A Novel Optical Integrate and Dump Receiver for Clocking Signals

[1]CEA LETI, [2]IEF

7A5 *Maciej Kucharski*, *Frank Herzel* and *Dietmar Kissinger*

Time-Domain Simulation of Quantization Noise Mixing and Charge Pump Device Noise in Fractional-N PLLs

IHP

10:30-12:00 Session 7B: EDA/CAD tools

LOCATION: Room 222

SESSSION CHAIRS: P. Desgreys - *Telecom Paristech*; M. Boukadoum - *UQAM*

7B1 *Michele Spasaro*[1], *Federico Alimenti*[2] and *Domenico Zito*[3]

A Black-Box Approach to RF LNA Design

[1]Università degli Studi di Perugia / Tyndall National Institute, [2]University of Perugia, [3]University College Cork

7B2 *Ehsan Ali*[1], *Wenceslas Rahajandraibe*[1], *Ndiogou Tall*[1], *Fayrouz Haddad*[1], *Christian Hangmann*[2] and *Christian Hedayat*

Modeling & PVT Characterization of arbitrary ordered VSCP- PLL using an Efficient Event-Driven Approach

[1]M2NP, Aix-Marseille University, Marseille, [2]University of Paderborn, [3]Fraunhofer ENAS

7B3 *Fu-Chiung Cheng*, *An-Hao Peng*, *Xiao-Li Lin* and *Shu-Chuan Huang*

Hybrid Encoded QDI Combinational Circuits

Tatung University

7B4 *Gabor Varga*, *Arun Ashok*, *Iyappan Subbiah*, *Moritz Schrey* and *Stefan Heinen*

A Workaround to the Higher Order Derivative Issue of Threshold Voltage Based MOSFET Models

RWTH Aachen University

7B5 *Carlo Pinciroli*, *Sami Riahi* and *Giovanni Beltrame*

A Low-Cost Validation Setup for the Thermal Modelling of Electronic Devices

MIST, École Polytechnique de Montréal

10:30-12:00 Session 7C: DSP and Multimedia Circuits and Applications

LOCATION: Room 224

SESSSION CHAIR: S. Bampi – *UFRGS, Y. Savaria – Polytechnique Montréal*

7C1 *Abdallah Meraoumia*[1], *Salim Chitroub*[2] and *Ahmed Bouridane*[3]

An Automated Ear Identification System Using Gabor Filter Responses

[1]Université Kasdi Merbah, [2]Electronics and Computer Science Faculty USTHB,[3]Northumbria University

7C2 *Roya Alizadeh*, *Normand Bélanger*, *Yvon Savaria* and *Jean-François Frigon*

DPDK and MKL; Enabling Technologies for Near Deterministic Cloud-based Signal Processing

Ecole Polytechnique de Montreal

7C3 *Cláudio Diniz*[1], *Mateus Fonseca*[2], *Eduardo Costa*[2] and *Sergio Bampi*[1]

Enhancing a HEVC Interpolation Filter Hardware Architecture With Efficient Adder Compressors

[1]Universidade Federal do Rio Grande do Sul, [2]Universidade Federal de Pelotas

7C4 *Yalcin Balcioglu* and *Gunhan Dundar*

A Synthesizable Time to Digital Converter (TDC) with MIMO spatial oversampling method

Bogazici University

12:00-14:00 Lunch Break

14:00-15:30 Session 8A: Noise and Random Phenomena in Analog Circuits

LOCATION: Auditorium

SESSSION CHAIR: D. Demarchi – *Politecnico di Torino, J.-P. Walder – IM2NP*

8A1 *Satoshi Oosawa*[1], *Takayuki Konishi*[1], *Naoya Onizawa*[2] and *Takahiro Hanyu*[1]

Design of an STT-MTJ Based True Random Number Generator Using Digitally Controlled Probability-Locked Loop

[1]Tohoku Univ., [2]University of Waterloo

8A2 *Francois Gaugaz*, *Francois Krummenacher* and *Maher Kayal*

High-Speed Analog Processing for Real-Time Fault Location in Electrical Power Networks

EPFL

8A3 *Assim Boukhayma*[1] and *Christian Enz*[2]

A New Method for kTC Noise Analysis in Periodic Passive Switched-Capacitor Networks

CEA-LETI, EPFL

8A4 *Mellouli Dorra*[1], *Cordeau David*[2] and *Mnif Hassene*

A Fully Integrated 5.78 GHz Array of two Differential Oscillators Coupled Through a MOS transistor Network

[1]University of Sfax, [2]Laii laboratory University of Poitiers

8A5 *Ali Nikoofard*, *Siavash Kananian* and *Ali Fotowat-Ahmady*

Analysis of the Effects of Clock Imperfections in N-Path Filters

[1]Sharif University of Technology

14:00-15:30 Session 8B: Digital Circuits and Architectures for Processing

LOCATION: Room 222

SESSION CHAIRS: A. Amara - *ISEP*, R. Possamai Bastos - *TIMA*

8B1 *Ali Ibrahim*, *Maurizio Valle*, *Hussein Chible* and *Luca Noli*

Singular Value Decomposition FPGA Implementation for Tactile Data Processing

University of Genova

8B2 *Leonardo Bandeira Soares*[1], *Eduardo Antônio Cesar Da Costa*[2] and *Sergio Bampi*[1]

Approximate Adder Synthesis for Area- and Energy- Efficient FIR Filters in CMOS VLSI

[1]UFRGS, [2]Catholic University of Pelotas

8B3 *Hanieh Abdollahifakhr*, *Normand Bélanger*, *Yvon Savaria* and *François Gagnon*

Power-Efficient Hardware Architecture for Computing Split-Radix FFTs on Highly Sparsed Spectrum

Ecole polytechnique de Montreal

8B4 *Lei Wu* and *Ching Chuen Jong*

A Curve Fitting Approach for Non-Iterative Divider Design with Accuracy and Performance Trade-off

Nanyang Technological University

8B5 *Kazunari Kato*, *Yasuhiro Takahashi* and *Toshikazu Sekine*

A 4×4-bit Multiplier LSI Implementation of Two Phase Clocking Subthreshold Adiabatic Logic

Gifu University

14:00-15:30 Session 8C: Energy Harvesting: from Devices to Systems

LOCATION: Room 224

SESSION CHAIR: J.-M. Duchamp - *IMEP-LAHC,* R. Vauché – *IM2NP*

8C1 *Iyappan Subbiah*[1], *Nashwa Abo Elneel*[2], *Gabor Varga*[1], *Arun Ashok*[1] and *Dietmar Schroeder*[2]

Low Power On-Chip Load Tracking-Zero Compensation Method for Low Dropout Regulator

[1]RWTH, [2]Hamburg University of Technology

8C2 *Nithin Jose*[1], *Nirmal John*[1], *Prashuk Jain*[2], *Prashant Raja*[1], *T.V Prabhakar*[1] and *K.J Vinoy*[1]

RF powered Integrated System for IoT Applications

[1]Indian Institute of Science, [2] Texas Instruments India Pvt. Ltd.

8C3 *Ayman Eltaliawy*, *Hassan Mostafa* and *Yehea Ismail*

A New Digital Locking MPPT control for Ultra Low Power Energy Harvesting Systems

The American University in Cairo

8C4 *David Cavalheiro*[1], *Francesc Moll*[1] and *Stanimir Valtchev*[2]

Tunnel FET device characteristics for RF energy harvesting passive rectifiers

[1]Univ. Politecnica de Catalunya, [2]University New of Lisbon - Faculty of Sciences and Technology

8C5 *Sebastien Boisseau*, *Pierre Gasnier*, *Matthias Perez*, *Matthias Geisler*, *Alexandre-Benoit Duret* and *Jerome Willemin*

Synchronous Electric Charge Extraction for Multiple Piezoelectric Energy Harvesters

CEA LETI

15:30-16:30 Coffee Break

15:45-17:00 Session 9A: Poster Session I

LOCATION: Grand Salon

SESSION CHAIR: Y. Deval - *IMS*

9A2 *Swetha George*, *Roland Cheng* and *Zeljko Ignjatovic*

A Novel Ultrasound Imaging Technique for Portable and High Speed Imaging

University of Rochester

9A3 *Gonenc Berkol*[1], *Ahmet Unutulmaz*[1], *Engin Afacan*[1], *Gunhan Dundar*[1], *Fransisco V. Fernandez*[2] *Ali Emre Pusane*[1] and *Faik Baskaya*[1]

A Two-Step Layout-in-the-loop Design Automation Tool

[1]Bogazici University, [2]IMSE

9A4 *Yu Bao*[1], *Jef Stals*[2], *Bart Stukken*[2], *Caikou Chen*[1] and *Luc Claesen*[2]

Quantitative Comparison of Lossless Video Compression for Multi-Camera Stereo and View Interpolation Applications

[1]Yangzhou University, [2]Hasselt University

9A5 *Tekfouy Lim*[1], *Luca Santarelli*[2], *Franco Cacialli*[2] and *Horst Gieser*[1]

ESD sensitivity investigation on P3HT thin film transistors

[1]Fraunhofer EMFT, [2]University College London

9A6 *Rengarajan Ragavan*[1], *Cedric Killian*[2] and *Olivier Sentieys*[2]

Low Complexity On-Chip Distributed DC-DC Converter for Low Power WSN nodes

[1]University of Rennes, [2]IRISA

9A7 *Truong Nguyen-Ly*[1], *Khoa Le*[2], *Fakhreddine Ghaffari*[2], *Alexandru Amaricai*[3], *Oana Boncalo*[3], *Valentin Savin*[1] and *David Declercq*[2]

FPGA Design of High Throughput LDPC Decoder based on Imprecise Offset Min-Sum Decoding

[1]CEA-LETI, [2]ETIS/ ENSEA, [3]Universitatea 'Politehnica' Timisoara

9A8 *Ali Sadr* and *Nasser Masoumi*

Bandwidth Enhancement of Planar EBG Structure Using Dissipative Edge Termination

University of Tehran

9A9 *Gaël Kamdem De Teyou*, *Hervé Petit* and *Patrick Loumeau*

Adaptive and Digital Blind Calibration of Transfer Function Mismatch in Time-Interleaved ADCs

Telecom ParisTech

9A10 *Matthieu Verdy*[1], *Dominique Morche*[1], *Suzanne Lesecq*[1], *Jean-Pascal Mallet*[2], *Cédric Mayor*[2] and *Emeric De Foucauld*[1]

Balancing Test Cost Reduction and Measurements Accuracy at Test Time

[1]CEA LETI, [2]PRESTO-ENGINEERING

9A11 *Lounis Zerioul*, *Myriam Ariaudo* and *Emmanuelle Bourdel*

Optimization of Spectral Resources Allocation in a Context of RF Network on Chip

ETIS/ ENSEA

9A12 *Ata Khorami*, *Mohammad Sadegh Espanah* and *Mohammad Sharifkhani*

Zero-Power Mismatch-Independent Digital to Analog Converter

Sharif University of Technology

9A13 *Zahra Katbay*[1], *Sawsan Sadek*[1], *Raafat Lababidi*[2], *Andre Perennec*[3] and *Marc Le Roy*[3]

Miniature Antenna for Breast Tumor Detection

[1]Lebanese university, [2]Ensta Bretagne, [3]UBO

9A14 *Farouk Amish*[1] and *El-Bay Bourennane*[2]

A Novel Hardware Accelarator for the HEVC Intra Prediction

[1]University of burgundy, [2]Le2i laboratory

9A15 *Raphael Vansebrouck*[1,2], *Olivier Jamin*[1], *Patricia Desgreys*[2] and *Van-Tam Nguyen*[2]

Digital distortion compensation for wideband direct digitization RF receiver

[1]NXP Semiconductors, [2] Telecom-ParisTech

9A16 *David Roma*[1], *José Bosch*[1], *Manuel Carmona*[1], *Albert Casas*[1], *Atilà Herms*, *José M. Gómez*[1], *Manel López*[1], *Josep Sabater*[1], *Jörg Baumgartner*[2], *Thorsten Maue*[2], *Wolgang Schmidt*[2] and *Reiner Volkmer*[2]

A space grade camera for image correlation

[1]University of Barcelona, [2]Kiepenheuer-Institut für Sonnenphysik

9A17 *Fernando Cruz-Roldán*[1], *Freddy Pinto-Benel*[1], *María Elena Domínguez-Jiménez*[2] and *Gabriela Sansigre Vidal*[2]

Single-Carrier Frequency Division Multiple Access with Discrete Cosine Transform Type-I

[1]University of Alcalá, [2]Universidad Politécnica de Madrid

9A18 *Chao Chu*, *Jens Anders*, *Joachim Becker* and *Maurits Ortmanns*

Finite GBW Compensation Technique for CT Delta-Sigma Modulators with Differentiator Based ELD Compensation

University of Ulm

9A19 *Weidong Cao*

A 40Gb/s 27mW 3-tap Closed-loop Decision Feedback Equalizer in 65nm CMOS

Institute of Microelectronics, Tsinghua University

15:45-17:00 Session 9B: Meiji University Students' workshop

LOCATION: Grand Salon

9B1 *Nur Alyaa Alias*, *Kosuke Tsumura* and *Tetsushi Ikegami*

Evaluation of BER in Different Location of Relay Nodes in Cooperative Transmission for Reliable Wireless Communication in Interference-Limited Environment

Meiji University

9B2 *Kenta Amino*, *Kawori Sekine*, *Kazuyuki Wada* and *Moriya Nakamura*

1.0V analog FIR filter design using inverters and gilbert cells with 28-nm FDSOI process

Meiji University

9B3 *Yu Daimon* and *Kazuyuki Wada*

Design of a Hysteretic Control COT Buck Converter

Meiji University

9B4 *Hiroyuki Imai* and *Kazuyuki Wada*

Effect of Aliase in a Direct Sampling Mixer with Complex Poles

Meiji University

9B5 *Yoshitaka Kitani*, *Kayuzuki Wada*, *Kawori Sekine* and *Moriya Nakamura*

Matching Circuits of Tapped Delay Line for the Transversal Filter

Meiji University

9B6 *Nobuaki Mitsuya* and *Kawori Sekine*

8GHz Voltage Controlled Oscillators with MOS varactor in 0.18-um CMOS Process

Meiji University

9B7 *Yuma Shimamura* and *Tetsushi Ikegami*

A Study on Human Body Detection while Walking by using SISO-UWB Radar in an Indoor Environment

Meiji University

9B8 *Tomoyuki Shiraki* and *Tetsushi Ikegami*

Link budget study of a radio relay system using unmanned aerial vehicles

Meiji University

9B9 *Chihiro Sudo*, *Akira Kashiwagi* and *Kazuyuki Wada*

Examination of Differential Amplifiers Based on Logic Gates

Meiji University

9B10 *Daiki Yamazaki* and *Kawori Sekine*

Improvement of temperature characteristics of the current mirror using subthreshold P-MOSFET

Meiji University

9B11 *Suguru Yasuraoka* and *Tetsushi Ikegami*

920MHz Indoor Propagation Measurement and Evaluation for Wireless Sensor Networks

Meiji University

9B12 *Dajana Danilovic*, *Andrei Vladimirescu*[1,2], *Andreia Cathelin*[3] and *Borivoje Nikolic*[2]

Low power RF receiver front-end evaluation in 28nm UTBB FDSOI

[1]ISEP, Paris, France, [2]BWRC, University of California, Berkeley, CA, [3]STMicroelectronics, Crolles, France.

9B13 *Milovan Blagojevic*, *Andrei Vladimirescu*[1,2], *Bora Nikolic*[2] and *Philippe Flatresse*[3]

Run-time Energy-Efficiency Optimization with Embedded Body-Bias Generator in 28nm UTBB FD-SOI Technology

[1]ISEP, Paris, France, [2]BWRC, University of California, Berkeley, CA, [3]STMicroelectronics, Crolles, France.

16:30-18:00 Session 10A: Special Session Circuits and Systems for Medical Applications

LOCATION: Auditorium

SESSION CHAIR: G. Charvet - *CEA*

10A1 *Lydia Chioukh*[1], *Dominic Deslandes*[2] and *Ke Wu*[1]

Low-Power Radar Techniques for Remote Sensing and Detection of Vital Signs

[1]Polytechnique Montréal, [2]Université du Québec À Montréal

10A2 *Guillaume Charvet*

A wireless fully implantable ECoG recording medical device WIMAGINE®: from the design of an integrated circuit toward a clinical trial

CEA-LETI-CLINATEC

10A3 *David Guiraud*[1], *C. Mestais, F. Sauter-Starace, M. Foerster, A. Lambert, C. Chabrol, S. Robinet, R. D'Errico, V. Josselin, N. Torres-Martinez, T. Costecalde, D. Ratel, A.L. Benabid*

Advanced Active Implantable Medical Devices how to get the best trade off between research needs and clinical usability

[1]CEA

16:30-18:20 Session 10B: Special Session On-chip Measurements for Characterization, Testing, and Calibration of Analog Front-ends and mmW Devices

LOCATION: Room 222

SESSION CHAIR: J.-D. Arnould, *IMEP-LAHC*

10B1 *Martin Andraud, Haralampos-G. Stratigopoulos, Emmanuel Simeu*

Self-healing of RF Circuits using Built-in Non-intrusive Sensors

TIMA

10B2 *Alice Bossuet*[1, 2,3], *Thomas Quémerais*[3], *Estelle Lauga-Larroze*[2], *Jean-Michel Fournier*[2], *Christophe Gaquière*[1] and *Daniel Gloria*[3]

150 GHz load pull measurements on BiCMOS 55nm SiGe:C HBT using in situ tuner

[1]IEMN, [2]IMEP-LAHC, [3]STMicroelectronics

10B3 *Luca Galatro* and *Marco Spirito*

Calibration and Characterization Techniques for On-Wafer Device Characterization

TU Delft

10B4 *Jinbo Wan* and *Hans Kerkhoff*

Embedded Instruments for Enhancing Dependability of Analogue and Mixed-Signal IPs

University of Twente / CTIT-TDT

10B5 *Dietmar Kissinger[1], Johannes Nehring[2], Andreas Oborovski[3], Karl Borutta[2], Ismail Nasr[4], Benjamin Laemmle[5]* and *Robert Weigel[3]*

Integrated Test Concepts for In-Situ Millimeter-Wave Device Characterization

[1]IHP, [2]FAU Erlangen-Nürnberg, [3]Institute for Electronics Engineering, [4]Infineon Technologies, [5]Intel

10B6 *Sebastien Fregonese[1,2], Rosario D'esposito[1,2], Magali De Matos[1,2], Andreas Köhler[3], Cristell Maneux[1,2] and Thomas Zimmer[1,2]*

Substrate-Coupling effect in BiCMOS technology for millimeter wave applications

[1]CNRS, [2]Université de Bordeaux, [3]Franhöfer Institute Dresden

18:45-21:00 Cocktail/ Museum visit

Tuesday, June 9th

09:00-10:00 Session 11: Plenary Lecture C. Fourtet (SigFox)

LOCATION: Auditorium

SESSION CHAIR: D. Morche – *CEA-LETI*

Christophe Fourtet

The technical challenges of future IoT networks and their consequences on modem's and SoC's design

SigFox

10:00-10:30 Coffee Break

10:00-11:30 Session 12A: Poster Session II

LOCATION: Grand Salon

SESSION CHAIR: H. Barthélemy – *IM2NP*

12A1 *Parinaz Hadadtehrani*, *Pouya Kamalinejad*, *Reza Molavi* and *Shahriar Mirabbasi*

An Adaptive Magnetically-Coupled Wireless Power Transmission System

University of British Columbia

12A2 *Salih Ergun*

Attack on a Chaos-Based "True" Random Bit Generator

ERARGE - Ergünler

12A3 *Michel Vasilevski*[1], *Eridenes Queiroz*[1], *Adauto Luis Fonseca*[2], *Sebastian Yuri Catunda*[1] and *Luiz Affonso H. Guedes de Oliveira*[1]

SystemC AMS Modeling of a Sensor Node Energy Consumption and Battery State-of-Charge for WSN

[1]Federal University of Rio Grande do Norte, [2]Potychip

12A4 *Laurent Fiack*, *Laurent Rodriguez* and *Benoît Miramond*

Hardware design of a Neural Processing Unit for bio-inspired computing

ETIS lab UMR 8051 CNRS / ENSEA / UCP

12A6 *Essia Ben Abdallah*, *Alexandre Giry*, *Serge Bories*, *Dominique Nicolas* and *Christophe Delaveaud*

Impact of Small Antenna on Linear Power Amplifier Performance in a Co-design Approach

CEA-LETI

12A7 *Christophe Layer*[1,3], *Kotb Jabeur*[1,3], *Stephane Gros*[2], *Laurent Becker*[1], *Pierre Paoli*[1,3], *Fabrice Bernard-Granger*[1,3], *Virgile Javerliac*[1,3] and *Bernard Dieny*[3]

Low-Power Hybrid STT/CMOS System-on-Chip Embedding Non-Volatile Magnetic Memory Blocks

[1]*CEA*, [2]*eVaderis*, [3]*SPINTEC*

12A8 *Khaled Mohamed*

New TSV-Based Applications: Resonant Inductive Coupling, Variable Inductor, Power Amplifier, Bandpass Filter, and Antenna

Mentor Graphics

12A9 *Emilie Avignon-Meseldzija*[1], *Pietro Maris Ferreira*[1], *Konstantinos Lekkas*[1] and *Fabrice Boust*[2]

A high-Q Tunable Grounded Negative Inductor for Small Antennas and Broadband Metamaterials

[1]*Supélec*, [2]*ONERA*

12A10 *Arthur Arnaud*[1], *Jihane Boughaleb*[1,2], *Stephane Monfray*[1], *Frederic Boeuf*[1] and *Orphee Cugat*[3]

Reduced model for the comprehension of the operation of a thermo-mechanical energy harvester

[1]*STMicroelectronics*, [2]*LGEF*, [3]*G2ELab*

12A11 *Hassan Anwar*, *Giovanni Beltrame* and *Chao Chen*

A Probabilistically Analysable Cache Implementation on FPGA

Ecole *Polytechnique de Montreal*

12A12 *Susan Schober* and *John Choma*

A Capacitively Phase-Coupled Low Noise, Low Power 0.8-to-28.2GHz Quadrature Ring VCO in 40nm CMOS

University of Southern California

12A13 *Kyle Fricke*, *Mengye Cai* and *Robert Sobot*

CMOS Voltage Regulator for RF Energy Harvester

The University of Western Ontario

12A14 *Elie Lefeuvre*[1], *Jie Wei*[1,2], *Hervé Mathias*[1,2] and *François Costa*[3]

Single-Switch Inductorless Power Management Circuit for Electrostatic Vibration Energy Harvesters

[1]*Université Paris Sud,* [2]*CNRS,* [3]*SATIE*

12A15 *Matthias Perez*, *Sebastien Boisseau*, *Pierre Gasnier*, *Jerome Willemin*, *Nicolas Pourchier*, *Matthias Geisler* and *Jean-Luc Reboud*

Electret-based Aeroelastic Harvester and its Self-starting Battery-free Power Management Circuit

CEA

12A16 *Vincent Lenoir*, *Warody Lombardi*, *Didier Lattard* and *Ahmed Jerraya*

Design and Implementation of a Closed-Loop Controller for a Self-Adaptive IEEE 802.15.4 DBB

CEA

12A17 *Athanasios Kiouseloglou*[1], *Gabriele Navarro*[1], *Alessandro Cabrini*[2], *Luca Perniola*[1] and *Guido Torelli*[2]

Optimized Temperature Profile Based Pulse Generator for Innovative Phase Change Memory

[1]*CEA-LETI,* [2]*University of Pavia*

12A18 *Mohamed Lamine Tounsi*[1], *Abdelhamid Khodja*[1] and *Mustapha C.E Yagoub*[2]

Dispersion Characteristics of Multilayered Anisotropic Microwave Circuits Independently of the Optical Axis Polarization

[1]*USTHB University,* [2]*University of Ottawa*

12A19 *Xufeng Wu*, *Yahui Leng*, *Lenian He* and *Jianxiong Xi*

A Linear Constant Current LED Driver without off-chip Inductor and Capacitor

Institute of VLSI Design, Zhejiang University

12A20 *Zhao Huatao*, *Su Xian* and *Takahiro Watanabe*

Application-Specific Shared Last-Level Cache Optimization for Low-Power Embedded Systems

Waseda University

12A21 *Sumedh Dhabu*, *Vinod A. P.* and *Madhukumar A. S.*

Low Complexity Fast Filter Bank-based Channelization in L-DACS1 for Aeronautical Communications

NTU

10:30-12:00 Session 13A: Timing Variations and Resiliency

LOCATION: Auditorium

SESSION CHAIR: L. Fesquet - *TIMA*

13A1 *Xinghua Yang*, *Fei Qiao*, *Qi Wei* and *Huazhong Yang*

A General Scheme for Noise-Tolerant Logic Design Based on Probabilistic and DCVS Approaches

Dept. of Electronic Engineering, Tsinghua University

13A2 *Gaetano Palumbo*[1], *Massimo Alioto*[2] and *Elio Consoli*[1]

Variability Budget in Pulsed Flip-Flops

[1]DIEEI - University of Catani, [2]University of Siena

13A3 *Delong Shang*, *Oyinkuro Benafa*, *Fei Xia*, *Alex Yakovlev* and *Yuqing Xu*

An Elastic Timer for Wide Dynamic Working Range

Newcastle University

13A4 *Joan Mauricio Ferré* and *Francesc Moll*

Local Variations Compensation with DLL-based Body Bias Generator for UTBB FD-SOI technology

Universitat Politècnica de Catalunya

13A5 *Mohamed Mohie El-Din*, *Hassan Mostafa* and *Yehea Ismail*

Performance Evaluation of FinFET-Based FPGA Cluster Under Threshold Voltage Variation

Cairo University

10:30-12:00 Session 13B: Modeling, Design and Conditioning of Sensing Devices

LOCATION: Room 222

SESSION CHAIR: L. Hébrard - *Université de Strasbourg*

13B1 *Matteo Maria Vignetti*[1], *Francis Calmon*[1], *Remy Cellier*[1], *Patrick Pittet*[1], *Laurent Quiquerez*[1] and *Aurore Savoy-Navarro*[2]

A time-integration based quenching circuit for Geiger-mode avalanche diodes

[1]Institut des Nanotechnologies de Lyon, [2]Laboratoire d'AstroParticule et Cosmologie, Université Paris-Diderot

13B2 *Laurent Osberger*, *Vincent Frick*, *Morgan Madec* and *Luc Hébrard*

High resolution, low offset Vertical Hall device in Low-voltage CMOS technology

ICube laboratory / University of Strasbourg

13B3 *Denis Sallin*, *Adil Koukab* and *Maher Kayal*

Optimized operation and temperature dependence of a direct Light-to-Time converter

EPFL

13B4 *Davide Marano* and *Alfio Dario Grasso*

A New Enhanced PSPICE Implementation of the Equivalent Circuit Model of SiPM Detectors

INAF - Osservatorio Astrofisico di Catania

13B5 *Imane Malass*, *Wilfried Uhring* and *Jean-Pierre Le Normand*

A Single Photon Avalanche Detector in a 180 nm standard CMOS technology

ICUBE, University of Strasbourg and CNRS

12:00-13:30 Lunch Break

13:30-15:00 Session 14A: Wireless Transmitters and Receivers

LOCATION: Auditorium

SESSION CHAIRS: D. Belot – *STMicroelectronics*; R. Sobot – *University of Western Ontario*

14A1 *Dajana Danilovic*[1], *Andreia Cathelin*[1], *Andrei Vladimirescu*[2] and *Borivoje Nikolic*[3]

Design considerations for Low Noise Transconductance Amplifiers in 28nm UTBB-FDSOI

[1]STMicroelectronics, [2]ISEP, [3]University of California, Berkeley

14A2 *José Ferreira*, *Jorge Fernandes* and *Hugo Gonçalves*

A 2.41 GHz ISM Receiver using an IQ VCO-Mixer

INESC-ID

14A3 *Jeffrey Walling* and *Wen Yuan*

A Switched-Capacitor Controlled Digital-Current Modulated Class-E EER Transmitter

University of Utah

14A4 *Zenggi Wang* and *Zhiqun Li*

A 1V 830μW Full-band ZigBee Receiver Front-end with Current-reuse and Gm-boosting Techniques

Southeast University

14A5 *Fikre Tsigabu Gebreyohannes*, *Antoine Frappé* and *Andreas Kaiser*

Semi-digital FIR DAC for Low Power Single Carrier IEEE 802.11ad 60GHz Transmitter

IEMN-ISEN

13:30-15:00 Session 14B: Mixed Signal Circuits

LOCATION: Room 222

SESSION CHAIRS: Erkan Isa - *EMFT;* He Tang - *Univ. of Electron. Science & Technol. of China*

14B1 *Mathieu Valleriani*[1], *Florin Hutu*[2], *Benoit Miscopein*[1], *Guillaume Villemaud*[2] and *Tanguy Risset*[2]

Additive Companding Implementation to Reduce ADC Constraints for Multiple signals Digitization

[1]Orange, [2]INSA Lyon CITI

14B2 *Jaswinder Lota*[1] and *Andreas Demosthenous*[2]

Q-enhancement with on-chip inductor optimization for reconfigurable delta-sigma radio-frequency ADC

[1]University of East London, [2]University College London

14B3 *Seok Min Jung* and *Janet Roveda*

A Low Jitter Digital Phase-Locked Loop With a Hybrid Analog/Digital PI Control

University of Arizona

14B4 *Amer Samarah* and *Anthony Chan Carusone*

Cycle-Slipping Pull-In Range of Bang-Bang PLLs

University of Toronto

14B5 *Claudio De Berti*[1], *Piero Malcovati*[1], *Lorenzo Crespi*[2] and *Andrea Baschirotto*[3]

Colored Clock Jitter Model in Audio Continuous-Time ΣΔ Modulators

[1]University of Pavia, [2]Conexant Systems, [3]Univ Milan Bicocca

15:00-15:20 Coffee Break

15:20-16:50 Session 15A: Voltage References and Power Converters

LOCATION: Auditorium

SESSION CHAIRS: W. Rahajandraibe – *IM2NP;* Tony Chan Carusone – *University of Toronto*

15A1 *David Cordova*[1], *Pedro Toledo*[1], *Hamilton Klimach*[2], *Sergio Bampi*[2] and *Eric Fabris*[1]

EMI Resisting MOSFET-Only Voltage Reference Based on the ZTC Condition

[1]NSCAD, [2]Federal University of Rio Grande do Sul,

15A2 *Omar Abdelfattah*[1], *Ishiang Shih*[1], *Gordon Roberts*[1] and *Yi-Chi Shih*[2]

A 0.6V-Supply Bandgap Reference in 65 nm CMOS

[1]McGill University, [2]University of California, Los Angeles

15A3 *Mohanad Ahmed* and *Mohammad Al-Ghamdi*

Rail-to-Rail Multiphase Supply Insensitive Voltage Controlled Oscillator for Low Power Converters

King Fahd University of Petroleum and Minerals

15A4 *Esmaeel Maghsoudloo*[1], *Masoud Rezaei*[1], *Mohamad Sawan*[2] and *Benoit Gosselin*[1]

A Power-Efficient Wide-Range Signal Level-Shifter

[1]Université Laval, [2]École Polytechnique de Montréal

15A5 *Vratislav Michal*, *Denis Cottin*, *Patrik Arno* and *Nicolas Marty*

Dual-phase 18V 280µA Charge Pump with Active Switches and Passive Level Shifter for Low-Voltage Capacitors

STMicroelectronics

15:20-16:50 Session 15B: Special Session Approximate Computing

LOCATION: Room 222

SESSION CHAIR: A. Amara - *ISEP*

15B1 *Shrikanth Ganapathy*[1], *Adam Teman*[1], *Robert Giterman*[2], *Andreas Burg*[3] and *Georgios Karakonstantis*[1]

Approximate Computing with Unreliable Dynamic Memories

[1]Ecole Polytechnique Federale de Lausanne, [2]Bar Ilan University, [3]ETH Zurich

15B2 *Vincent Camus*, *Jeremy Schlachter* and *Christian Enz*

Energy-Efficient Digital Design through Inexact and Approximate Arithmetic Circuits

EPFL

15B3 *Xun Jiao*[1], *Abbas Rahimi*[1], *Balakrishnan Narayanaswamy*[1], *Hamed Fatemi*[2], *Jose Pineda de Gyvez*[2] and *Rajesh Gupta*[1]

A Scalable Model for Timing Error Prediction under Hardware and Workload Variations

[1]University of California at San Diego, [2]NXP

15B4 *Leonardo Bandeira Soares*[1], *Sergio Bampi*[1], *André Luis Rodeghiero Rosa*[1] and *Eduardo Antônio Cesar Da Costa*[2]

Near-Threshold Computing for Very Wide Frequency Scaling: Approximate Adders to Rescue Performance

[1]*Federal University of Rio Grande do Sul,* [2]*Catholic University of Pelotas - UCPel*

15B5 *Lirida Naviner*[1], *Hao Cai*[1], *You Wang*[1], *Zhao Weisheng*[2] and *Arwa Ben Dhia*[1]

Stochastic Computation With Spin Torque Transfer Magnetic Tunnel Junction

[1]*Telecom ParisTech,* [2]*Univ. Paris-Sud*

16:50-18:10 Panel Session

IoT Revolution: What is the key enabler? Technology, Software or Application?

LOCATION: Auditorium

18:30 Gala Dinner Château de Sassenage

Wednesday, June 10th

09:00-10:30 Session 17A: Microwave and mm-wave Circuits

LOCATION: Auditorium

SESSION CHAIRS: J. M. Fournier – *IMEP-LAHC*; F. Nabki - *UQAM*

17A1 *Domenico Pepe*[1] and *Domenico Zito*[2]

A Compact 67 GHz Oscillator in 65nm CMOS

[1] *Tyndall National Institute,* [2] *University College Cork*

17A3 *Ekta Sharma*, *Alfredo Bautista*, *Emmanuel Pistono*, *Philippe Ferrari* and *Sylvain Bourdel*

81-86 GHz VCO for Backhaul application with S-CPS based differential Inductor in BiCMOS 55nm Technology

IMEP-LAHC

17A4 *Imen Ghorbel* and *Fayrouz Haddad*

Ultra Low Power RF Cross-Coupled VCO Design in the Subthreshold Regime with High Immunity to PVT Variations in 130nm CMOS technology

IM2NP

17A5 *Florent Torres*[1,2], *Jean-Baptiste Bégueret*[1], *Nicolas Martin*[1,2], *Didier Belot*[2] and *Thierry Taris*[1]

A Novel Tunable Impedance Transmission Line for mm-Waves Applications

[1] *IMS Bordeaux,* [2] *STMicroelectronics*

09:00-10:30 Session 17B: Building Blocks for Biomedical Applications

LOCATION: Room 222

SESSION CHAIR: E. Kussener – *IM2NP-ISEN Toulon*

17B1 *Mohammad Usaid Abbasi*[1], *Georgios Raikos*[2], *Ruchir Saraswat* [2] and *Esther Rodriguez-Villegas*[2]

A high PSRR, ultra-low power 1.2V curvature corrected Bandgap Reference for Wearable EEG application

[1] *University of Southampton,* [2] *Imperial College London*

17B2 *Francois Rummens*, *Sylvie Renaud* and *Noelle Lewis*

CMOS Differential Neural Amplifier with High Input Impedance

IMS - Bordeaux University

17B3 *Pere Llimós Muntal*[1], *Dennis Øland Larsen*[1], *Kjartan Færch*[2], *Ivan Harald*[1] *Holger Jørgensen*[1] and *Erik Bruun*[1]

Integrated Differential High-Voltage Transmitting Circuit for CMUTs

[1]Technical University of Denmark, [2]Analogic Ultrasound, BK Medical Design Center

17B4 *Yuwadee Sundarasaradula* and *Apinunt Thanachayanont*

A 1-V, 6-nW Programmable 4th-order Bandpass Filter for Biomedical Applications

King Mongkut's Institute of Technology Ladkrabang

17B5 *Robert Gallichan*[1], *Daniel McCormick*[2], *Rezaul Hasan*[3], *Patrick Hu*[1] and *David Budgett*[2]

Analysis of Peak Currents in Integrated Synchronous Rectifiers

[1]University of Auckland, [2]Auckland Bioengineering Institute, [3]Massey University Albany

09:00-10:30 Session 17C: Analog-to-Digital Converters

LOCATION: Room 224

SESSION CHAIRS: M. de Matteis – *Unimib*; P. Loumeau – *Télécom ParisTech*

17C1 *Chithira Ravi*, *Vineeth Sarma* and *Bibhudatta Sahoo*

At Speed Digital Gain Error Calibration of Pipelined ADCs

Amrita Vishwa Vidyapeetham

17C2 *Weitao Li*, *Fule Li*, *Ya Wang*, *Chun Zhang* and *Zhihua Wang*

A Power-Efficient 14-bit 250MS/s Pipelined ADC

Tsinghua university

17C3 *Li Shengjing*, *Li Weitao* and *Li Fule*

A Digital Blind Background Calibration Algorithm for Pipelined ADC

Tsinghua University

17C4 *Luca Giuffredi*[1], *Giorgio Pietrini*[1], *Marco Ronchi*[2], *Alessandro Magnanini*[3] and *Andrea Boni*

Low-Power 3rd order Sigma Delta Modulator in CMOS 90-nm for sensors interface applications

[1]*Universtà degli studi di Parma,* [2]*STMicroelectronics,* [3]*Silis s.r.l,*

17C5 *Ahmed Hamza*[1], *Sameh Ibrahim*[1], *Mohamed El-Nozahi*[1]and *Mohamed Dessouky*[2]

A Low-Power, 9-Bit, 1.2 ps Resolution Two-Step Time-to-Digital Converter in 65 nm CMOS

[1]*Ain Shams University,* [2]*Mentor Graphics Egypt*

10:30-10:50 Coffee Break

10:50-11:50 Session 18: Plenary Lecture B. Nauta

LOCATION: Auditorium

SESSION CHAIR: P. Desgreys – *Telecom Paristech*

Bram Nauta

Circuit Techniques for next Generation Wireless Communication

University of Twente

11:50-13:30 Lunch Break

13:30-15:00 Session 19A: Circuits for Wireless Communications

LOCATION: Auditorium

SESSION CHAIR: J. L. Gonzalez Jiménez – *CEA Leti,* Sylvain Bourdel – *IMEP-LAHC*

19A1 *Marcelo De Souza*[1], *André Mariano*[2] and *Thierry Taris*[3]

Inductorless Low Power Wideband LNA in 130 nm CMOS

[1]*UTFPR,* [2]*DELT - GICS – UFPR,* [3]*Université de Bordeaux I*

19A2 *Parvaneh Saffari*[1], *Mohammad Taherzadeh Sani*[1], *Ali Basaligheh*[2], *Frederic Nabki*[3] and *Mohamad Sawan*[4]

Low-Energy CMOS Common-Drain Power Amplifier for Short-Range Applications

[1]*Ferdowsi University of Mashhad,* [2]*ETS Montreal,* [3]*Université du Québec à Montréal,* [4]*Ecole Polytechnique de Montréal*

19A3 *Remy Vauche*[1], *Eloi Muhr*[1], *Ndiogou Tall*[1], *Abderrahmane Haloua*[1], *Sylvain Bourdel*[2], *Jean Gaubert*[1], *Nicolas Dehaese*[1] and *Herve Barthelemy*[1]

Ultra-WideBand Voltage Controlled Oscillator with Commutable Phases for BPSK Implementation

[1]Aix-Marseille University - IM2NP, [2]IMEP-LAHC

19A4 *Răzvan Cristian Marin*[1], *Antoine Frappé*[1], *Andreas Kaiser*[1] and *Andreia Cathelin*[2]

Considerations for High-Speed Configurable-bandwidth Time-interleaved Digital Delta-Sigma Modulators and Synthesis in 28 nm UTBB FDSOI

[1]IEMN-ISEN, [2]STMicroelectronics

19A5 *Ayssar Serhan*, *Estelle Lauga-Larroze* and *Jean-Michel Fournier*

Efficiency Enhancement Using Adaptive Bias Control for 60GHz Power Amplifier

IMEP-LAHC

13:30-15:00 Session 19B: Systems for Biomedical Applications

LOCATION: Room 222

SESSION CHAIR: S. Mirabbasi - *University of British Columbia*

19B1 *Wout Swinkels*[1], *Yi Sun*[2], *Bart Stukken*[1], *Constantinus Politis*[1] and *Luc Claesen*[1]

Cloud-based Orthognathic Surgical Planning Platform

[1]University Hasselt, [2]KU Leuven

19B2 *Xusheng Wang*[1], *Ming Zhang*[1], *Xiaojiao Ren*[1], *Francis Rodes*[2] and *Romain Deniéport*[2]

Auto Tuning System for a Half Bridge Resonant Converter Using a Synchronous Switched Capacitor

[1]University of South Paris 11, [2]ENSEIRB-MATMECA

19B3 *Masoud Rezaei*[1], *Esmaeel Maghsoudloo*[2], *Mohamad Sawan*[3] and *Benoit Gosselin*[1]

A Novel Multichannel Analog-to-Time Converter Based on a Multiplexed Sigma Delta Converter

[1]Université Laval, [2]LRTS, [3]École Polytechnique de Montréal

19B4 *Pankaj Kumar Jha*[1], *Pravanjan Patra*[2], *Jairaj Naik*[1], *Ashudeb Dutta*[1], *Amit Acharya*[1], *Shiv Govind Singh*[1] and *P. Rajalakshmi*[1]

A 2µW Biomedical Frontend with ADC for Self-powered u-Healthcare Devices in 0.18µm CMOS

[1]IIT Hyderabad, [2]National Institute of Technology,

19B5 *Muriel Muller* and *Ghalid Abib*

Ultra WideBand RADAR System for Human Chest Displacement

Telecom Sud Paris

13:30-15:00 Session 19C: Special Session Control Techniques for Adaptive Computing Systems

LOCATION: Room 224

SESSION CHAIR: S. Lesecq – *CEA-Leti*

19C1 *Yeter Akgul*[1], *Diego Puschini*[1], *Lionel Vincent*[2], *Pascal Benoit*[3] and *Mauricio Altieri*[1]

Energy-efficient control through power mode placement with discrete DVFS and Body Bias

[1]CEA LETI, MINATEC Campus, [2]PERSYVAL-Lab, [3]LIRMM, University of Montpellier 2

19C2 *Benedikt Janßen*, *Fynn Schwiegelshohn* and *Michael Hübner*

Adaptive Computing in Real-Time Applications

Ruhr-University Bochum

19C3 *Mykhailo Zarudniev*[1], *Arnaud Tonda*[1], *Laurent Alacoque*[1], *Sebastien Bolis*[2], *Fabrice Jacquet*[1] and *Arnaud Pouydebasque*[2]

Autofocus performance realization using automatic control approach

[1]CEA-LETI, [2]Wavelens

19C4 *Chuan Shan*[1], *Eldar Zianbetov*[2], *François Anceau*[1], *Olivier Billoint* and *Dimitri Galayko*[1]

A distributed synchronization of all-digital PLLs network for clock generation in synchronous SOCs

[1]UPMC,[2]CEA INAC-SPINTEC

19C5 *Olesia Mokrenko*[1], *Maria Isabel Vergara-Gallego*[1], *Warody Lombardi*[1], *Suzanne Lesecq*[1] and *Carolina Albea*[2]

WSN Power Management with Battery Capacity Estimation

[1]CEA-LETI, [2]Univ. de Toulouse LAAS-CNRS

15:00-15:20 Coffee Break

15:20-16:50 Session 20A: Digital Design and Modeling

LOCATION: Auditorium

SESSION CHAIR: M. Belleville – *CEA-Leti*

20A1 *Gaspard Hiblot*[1], *Quentin Rafhay*[2], *Frédéric Boeuf*[1] and *Gérard Ghibaudo*[2]

Impact of short-channel effects on velocity overshoot with hydrodynamic transport

[1]STMicroelectronics, [2]IMEP-LAHC

20A3 *Khaled Helal*, *Sameh Attia*, *Tawfik Ismail* and *Hassan Mostafa*

Priority-Select Arbiter: An Efficient Round-Robin Arbiter

Cairo University

20A4 *Mickaël Fiorentino*[1], *Yvon Savaria*[1], *Omar Al-Terkawi*[1] and *Claude Thibeault*[2]

Self-Timed Circuits FPGA Implementation Flow

[1]École Polytechnique de Montréal, [2]Ecole des Technologies Supérieures Montréal

20A5 *Florent Berthier*[1], *Edith Beigne*[1], *Pascal Vivet*[1] and *Olivier Sentieys*[2]

Power Gain Estimation of an Event-driven Wake-Up Controller dedicated to WSN's Microcontroller

[1]CEA leti, [2]IRISA/INRIA

15:20-16:50 Session 20B: Filters and Transconductors

LOCATION: Room 222

SESSION CHAIR: T. Taris - *IMS*

20B1 *Astria Nur Irfansyah*[1], *Andrew Nicholson*[1], *Julian Jenkins*[2], *Tara Julia Hamilton*[3] and *Torsten Lehmann*[1]

Subthreshold Operation of Nauta's Operational Transconductance Amplifier

[1]School of Electrical Engineering and Telecommunications UNSW, [2]Perceptia Ltd, [3]University of Western Sydney

20B2 *Federica Resta*[1], *Marcello De Matteis*[1], *Alessandro Pezzotta*[1], *Stefano D'Amico*[2] and *Andrea Baschirotto*[1]

A 30MHz 28dBm-IIP3 3.2mW Fully-Differential Sallen-Key 4th-Order Filter with Out-of-Band Zeros Cancellation

[1]University of Milano-Bicocca, [2]University of Salento

20B3 *Hervé Barthelemy*[1], *Rémy Vauche*[2] and *Sylvain Bourdel*[3]

Digitally Controlled Transconductor Based on a Quantum Transconductance

[1]University of Toulon (UTLN), [2]Aix-Marseille University, [3]IMEP-LAHC

20B4 *Lucie Chandernagor*[1], *Patrick Jean*[1], *Bernard Jarry*[2] and *Julien Lintignat*[2]

Self calibrating High sensitivity Ultra-low power Envelope detector

[1]NXP Semiconductors, [2]XLIM

20B5 *Salvatore Pennisi*[1], *Alfio Dario Grasso*[1] and *Elena Cabrera-Bernal*[2]

0.7-V Bulk-Driven Three-Stage Class-AB OTA

[1]University of Catania, [2]University of Sevilla

15:20-16:50 Session 20C: Sensing Systems Integration

LOCATION: Room 224

SESSION CHAIR: W. Uhring - *University of Strasbourg*

20C1 *Luca Aluigi*[1] and *Domenico Zito*[2]

Analysis and Design of Ka-Band SoC Radiometer for Space Detection of Solar Flares

[1]Tyndall National Institute, [2]University College Cork

20C2 *Evgenia Voulgari*[1], *Matthew Noy*[2], *Francis Anghinolfi*[2], *Francois Krummenacher*[1] and *Maher Kayal*[1]

Sub-picoampere, 7-decade current to frequency converter for current sensing

[1]EPFL, [2]CERN

20C3 *Simon Paulus*[1], *Jean-Baptiste Kammerer*[1], *Joris Pascal*[2] and *Luc Hebrard*[1]

Continuous calibration of Rogowski coil current transducer

[1]ICube, [2]ABB Corporate Research

20C4 *Imane Malass*, *Wilfried Uhring* and *Jean Pierre Le Normand*

Efficiency improvement of high rate integrated Time Correlated Single Photon Counting systems by incorporating an embedded FIFO

ICUBE University of Strasbourg and CNRS

20C5 *Shigenori Yamauchi* and *Takamoto Watanabe*

All-digital MEMS tuning-fork self-excited vibration control by phase-relation using TAD-based ADPLL

DENSO CORPORATION

16:50-17:20 Closing Ceremony

LOCATION: Auditorium

14th IEEE International NEWCAS Conference
June 26 to 29, 2016
Vancouver, BC, Canada

On behalf of the organizing committee, we would like to take this opportunity to invite you to participate in the 14th IEEE International NEWCAS Conference, which will be held in Vancouver, BC, Canada from June 26 to 29, 2016. The venue for the conference will be Vancouver Marriott Pinnacle Downtown Hotel. With your participation, NEWCAS 2016 will continue the tradition of NEWCAS to have a rich mix of technical and social programs.

Facts about Vancouver:

"Vancouver is Manhattan with mountains. It's a liquid city, a tomorrow city, equal parts India, China, England, France and the Pacific Northwest. It's the cool North American sibling." — **The New York Times**

"Vancouver is a city unlike any other. Wherever I look, I see water or mountains -- or both. And everyone looks so healthy." — **The Daily Telegraph (UK)**

"With a vast multicultural population, endless activities, and excellent infrastructure, Vancouver is welcoming to all …. The Vancouver International Airport has consistently been rated as a top North American airport providing easy access from all over the world. Exceptional public transportation is overshadowed slightly by the convenience of Vancouver as a great walking city - clean, green, safe, and easily accessible!" — **Tourism Vancouver**

We are looking forward to welcoming you to NEWCAS 2016 in Vancouver.

13th IEEE International NEWCAS Conference

June 7-10, Grenoble, France